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(71) Applicant *(for all designated States except US)*: TELSTRA R & D MANAGEMENT PTY. LTD. [AU/AU]; 255 Elizabeth Street, Sydney, NSW 2000 (AU).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: HAWKINS, John, Maurice [AU/AU]; 6 Weeks Drive, Rowville, VIC 3178 (AU).

(74) Agents: WEBBER, David, Brian et al.; Davies Collison Cave, 1 Little Collins Street, Melbourne, VIC 3000 (AU).

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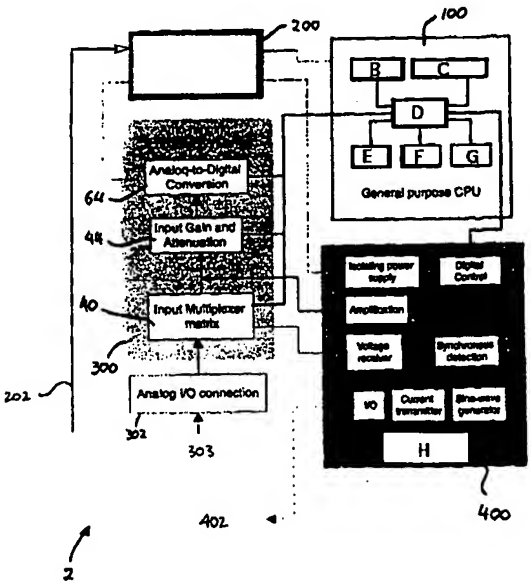

200...WIDE RANGE SWITCH MODE POWER SUPPLY (SMPS) 8V-100V
B...KEYPAD
C...LCD DISPLAY
D...CPU
E...RAM
F...RTC
G...ROM
H...IMPEDANCE MEASUREMENT

(57) Abstract

A monitoring system for monitoring parameters of an apparatus, comprising a plurality of inputs for receiving a plurality of electrical analog signals representative of parameters of the apparatus, a multiplexing circuit for multiplexing the analog signals into sequential analog input signals, an auto-ranging circuit for individually scaling each of the sequential analog input signals to within a predetermined range suitable for digital processing thereof, a signal converter for converting the scaled sequential analog input signals into respective digital signals, and digital processing system for storing and/or manipulating the digital signals.

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ELECTRICAL PARAMETER MONITORING SYSTEM

This invention relates to a system for monitoring electrical parameters. A particular application of the invention lies in the field of monitoring performance parameters of battery based or other power systems.

In many electrically operated systems, the integrity of the power supply is crucial to reliable operation, and this may include the integrity of a back-up power supply which is only actually utilised sporadically. An example is a telecommunications exchange installation, which ordinarily derives power from a mains supply connection, but is also provided with a battery based back-up power system to ensure the exchange can continue to operate in the event that the mains power should fail. The battery based power system is utilised only occasionally, however, it is nevertheless very important that it be continuously in a condition to enable it to power the telecommunications equipment at any time, since the loss of mains power cannot generally be predicted. Accordingly, various forms of testing apparatus have been developed in order to assess the condition of the batteries in the back-up power system, and one such form of testing apparatus is described in the specification of Australian Patent No. 688298. Typically, testing apparatuses of this type have been constructed so as to be portable, in order to be suitable to be carried by a service person from one installation to another for the purposes of periodic testing of the batteries at the installations.

Another approach to ensuring battery integrity involves continuous on-line monitoring. Commercially available battery monitoring systems typically involve broad-based surveillance of a relatively large number of batteries by centralised logging equipment. These systems are characteristically expensive and often require a secondary level or platform of support for the storage, processing and interpretation of collected data.

The present invention aims to provide a monitoring system which is flexible in its application and yet simple enough so that it can be implemented and operated at relatively low cost. It will be appreciated from the following description of the invention that the monitoring system

is not merely applicable to battery based power systems, although the preferred embodiment described herein is in that context. Indeed, the monitoring system of the invention is not restricted to power systems or in fact even to monitoring electrical apparatus, as long as analog electrical signals can be generated for input to the monitoring system.

In accordance with the present invention, there is provided a monitoring system for monitoring parameters of an apparatus, comprising:

a plurality of inputs for receiving a plurality of electrical analog signals representative of parameters of said apparatus;

a multiplexing circuit for multiplexing said analog signals into sequential analog input signals;

an auto-ranging circuit for individually scaling each of said sequential analog input signals to within a predetermined range suitable for digital processing thereof;

a signal converter for converting the scaled sequential analog input signals into respective digital signals; and

digital processing means for storing and/or manipulating said digital signals.

The present invention further provides a method for monitoring parameters of an apparatus, comprising the steps of:

receiving a plurality of electrical analog signals representative of parameters of said apparatus;

multiplexing said analog signals into sequential analog input signals;

scaling each of said sequential analog input signals to within a predetermined range suitable for digital processing thereof;

converting the scaled sequential analog input signals into respective digital signals using signal converter means; and

storing and/or manipulating said digital signals using digital processing means.

The present invention further provides a monitoring system, comprising:

an input means for receiving at least one electrical signal input;

a data acquisition means for obtaining first data values representing the at least one signal input repeatedly sampled at a first time interval;

a first storage means for storing said first data values;

a first averaging means for generating second data values representing averaged values of said first data values over a second time interval; and

a second storage means for storing said second data values

The present invention further provides a monitor for monitoring a battery, comprising:

battery impedance means for generating sampled impedance measurements of the impedance of said at least one battery at predetermined sampling intervals; and

storage means for storing digital representations of said sampled impedance measurements in a plurality of memory means, each memory means being adapted to store representations of said sampled impedance measurements generated at respective different time intervals.

The present invention further provides a method of monitoring a plurality of batteries or cells, comprising:

repeatedly measuring an impedance of each of said plurality of batteries or cells over a predetermined time interval;

recording digital representations of the measured impedances; and

determining, using said digital representations, a measure of a time differential of the impedance of each of the plurality of batteries or cells.

Advantageously, embodiments of the invention enable on-line or "live", determination of impedances on all individual battery cells or other components for which impedance measurements might be taken.

The invention is described in greater detail hereinafter, by way of example only, with reference to a preferred embodiment thereof which is illustrated in the accompanying drawings, wherein:

Figure 1 is a functional block diagram of a preferred embodiment of the invention, referred to herein as an intelligent monitoring system or IMS;

Figures 2 to 12 are circuit diagrams of interconnected components forming the IMS;

Figure 13 is a block diagram illustrating an input sampling arrangement according to one form of the invention;

Figure 14 is a flow diagram of the sampling procedure;

Figure 15 is a block diagram illustrating a storage system according to one form of the invention;

Figure 16 is a block diagram of the event recording functions of the IMS;

Figure 17 is a block diagram of primary functional software elements; and

Figure 18 is a block diagram illustrating the general input processing structure of the IMS.

A preferred embodiment of the present invention, referred to herein as an intelligent monitoring system (IMS), has been designed primarily for continuous monitoring of a power system, such as a battery based back-up power system for telecommunications exchanges and the like. Battery integrity is critical to the standby power function. Real-time continuous monitoring is considered to be part of the pathway to improved battery system reliability, particularly for installations using valve-regulated lead-acid (VRLA) battery technology. Integration of new techniques such as cell and battery impedance or conductance measurements has been advocated to both increase the efficacy of on-line monitoring systems, and to eliminate many of the problems associated with manual impedance measurement of on-line standby batteries.

The major influence in battery monitoring equipment functionality comes from considering the productivity of maintenance effort. The advantage of continuous monitoring to trap unattended events is obvious. The ability to track system performance during normal line failures is useful and may avoid the inconvenience and risks associates from routine test discharging.

However, the potential of monitors to guide corrective or proactive maintenance action is less evident. For instance, in a remote solar powered network, a low volts alarm may result in the dispatch of urgent maintenance action to recharge the batteries. The cause of the low battery capacity may not be evident, and this often results in costly, repeated call-outs. The reactive maintenance may be made more effective if the recent history of the power system performance parameters were at hand to help identify the cause of the under-charged condition.

The Intelligent Monitoring System, or IMS, is characterised by an "intelligent" balance between the data collection and storage activities (logging) and the system condition assessment tasks (monitoring). Each of the tasks can be allied with particular existing maintenance actions (or lack thereof). This concept lends itself well to power system monitors, not just battery monitors. Further, the IMS is independent of either the centralised or local status of the battery data collection activities associated with commercial battery monitoring systems.

The preferred form of the IMS results in very decoupled software and hardware. That is, the tasking software is functionality objective, and could easily execute on other hardware. This is an important outcome because many commercial battery monitoring systems lose some functionality because of inflexible coupling of operating software with the physical hardware. In the attempt to achieve a low cost, "universal" battery and power monitoring system, the parameters required to be monitored should be considered. The dilemma of what, how and why to measure in a battery monitoring system typically skews hardware design and selection. However, some gains can be made by firstly recognising that, for standby services, there is no genuine battery fuel gauge, and secondly, most of the conventional physical parameter measurements are historical in origin. From a pragmatic point of view, recently reported techniques indicate that better methods to determine critical battery "state-of-health" criteria can reasonably be expected in the future. It therefore follows that a newly developed battery monitoring system should preferably exhibit flexibility to accommodate changes to both the collection and utilisation of the parameter set.

The IMS is based on a generalised voltage input data acquisition design and does not limit the type of input parameter. There are, of course, limits placed on both the dynamic range of the voltage presented to the analog input multiplexer hardware, and the physical number of analog input channels available, but these limits need not affect the actual software tasking functionality. In a telecommunications network, the battery banks in the network exchanges might typically be based on a traditional 24×2V cell configuration, and this may therefore form a driving criterion for dynamic range and number of input channel limitations. Situations requiring more input channels, say for UPS applications or for multiple parallel battery banks, can be addressed by using more than one IMS. The major cost of a battery monitoring system is generally in the analog input acquisition circuitry, not in the support digital electronics. It is thus more cost effective to utilise multiple devices operating the same software than it is to have multiple input structures (to accommodate different battery installations) with associated variations in software.

In the IMS described herein, it will be recognised as significant by those skilled in the art that, for the purposes of the monitoring operations of the IMS, it is unimportant what voltage is presented at any one of the analog inputs, as long as it is smaller in magnitude than the maximum voltage rating of the input circuitry, since the input voltage range is independent of the voltage provided to the power supply of the IMS.

An attractive feature of the IMS is in the local event recording function performed primarily through the controlling software. Figure 16 illustrates the different types of event recording classes implemented in the preferred IMS. In practical terms, the Trend Tracker and Battery History classes relate to continuous logging activities, while the Discharge Logger and Exception Register relate more to random and unpredictable real-time events.

Each event type can be associated either directly or indirectly with one or more real inputs. As an example, Figure 17 illustrates in a functional sense how three different windows of trend tracking can be achieved within the IMS. Short-term, mid-term and long-term data describing system parameters and any derived information are available at any time. Table

1, below, lists typical time dimensions for these trend windows. For example, 8 hours of the most recent time sequential processed data, time-resolved to 5 minutes, is locally available for any and all of the defined inputs associated with the short-term trend. Similarly, the mid-term trend contains the most recent 8 day history, resolved to 1 hour. The long-term trend gives the most recent 30 day trend. Ultimately, the trend data is selectively filtered off into the Battery History register. The Battery History is the automation of the existing prescribed manual battery measurement routines, and as such can be described as the "electronic battery book". The Battery History data is protected, thus creating a local, electronic, permanent record of performance over the service life of the battery.

Trend Tracker	t sampling rate	T trend window	n no. of samples
short-term	5 min	8 hr	96
mid-term	1 hr	8 day	196
long-term	24 hr	30 day	30
Battery-History	30 day	unlimited	unlimited

Table 1: Typical trend window dimensions

The trend trackers in the preferred IMS comprise circular memory designs, and thus only the most recent trend data is locally available. This recognises that in relation to Table 1, storage of 5 minute samples for the life of the battery is both unreasonable and unnecessary. From an operational point of view, the more recent history information is most relevant. Connection of the IMS to a remote device provides a means to build an extended set of highly time-resolved data by retrieving data at a more frequent rate.

The surprising outcome of this approach is the relatively low rate of local memory consumption. The IMS can be implemented with only 64kB of RAM with less than 20% consumption per year of operation for the typical 24 cell battery installation using 30 day history records. Such low memory requirements reduce costs, limits the physical size and

enables useful local functionality without the need for centralised data collection.

The general specifications and features of a particular implementation of the IMS are given in Table 2, and some typical input parameter assignments are listed in Table 3. The preferred device has a 32 channel voltage input structure arising from modelling the 24×2V cell structure of the standard 48V battery bank installation. Other types of battery banks, except for UPS installations, can be modelled as a subset of the 24 cell situation. Generally, UPS installations require more numerous parameters to be monitored, but this can usually be accommodated by some integer multiple of 24 or 32. The input channels have a high common-mode voltage tolerance and an auto-ranging function ensures that there is no functional difference between 2V cells and 6V or 12V monoblocks.

Category	Description
Analog	32 differential channels
Input range	±160V (2000V isolation)
Scaling	Auto-ranging
A/D Conversion	13 bit 100 μsec, SAR ADC
Digital	68HC11 series 8 bit CPU
RAM	32K-128K non-volatile
ROM	128K UVEPROM (secure)
User interface	2-line LCD display and keypad
Remote access	Isolated RS-232 (9 pin)
Powering	Self-powered by monitored battery
Operating range	±8V-±100V, fully isolated
Power consumption	Approx. 1-2 Watt average
Physical	
Dimensions	104 (W) × 50 (H) × 270 (L) mm
Input loom	Universal 68 way mini-Centronics

Table 2: Some IMS hardware specifications

The IMS is self-powered from the battery installation under measurement and has very low power consumption. Collected data is memory protected. A standardised, "universal" input loom is utilised for all battery configurations. Intercell conduction integrity is directly

measured by a two wire per cell or monoblock connection scheme. The IMS can utilise a single frequency or multiple frequency impedance measurement as a core set of the battery and power system parameter set. Battery health information can be made on the basis of time trends in impedance measured at a single (same) frequency, or in changes in the ratio of impedance measurement at one frequency compared to another. Configuration options are software implemented, so that there are no hardware switches or settings, thus avoiding the need for field adjustment and the possibility of incorrect configuration.

The controlling "Software Construct" of the IMS is based upon an "owner-user" model in which the "owner" and "user" are responsible for different aspects of the IMS configuration and operation functions. The software functions as a rule-based expert system which is configurable by the "owner" to suit the application for which the particular IMS is intended. For example, because the IMS is constructed as a "universal" monitoring device, the plural physical inputs are undefined at the time of manufacture, and must be assigned some context before installation.

The software construct allows the IMS to identify classes of events, which relate to the physical state (status) of the system being monitored by the IMS (for example, in battery and power system monitoring, whether the system is in charge, discharge, or standby (float) condition). The occurrence of an event (transition between one state to another) is recorded by the IMS for the life of the installation. This is important in analysis of conditions which may result in an exception, as well as providing statistics about the operation of the systems which would otherwise not be recorded with current practises or with traditional types of battery monitors. Information gathered during an event is used by the expert system rule book to build a picture of the health of the system. For instance, if during a charge event, the time for charge of one or more cells is unreasonably long, then those cells are indicated to be of poor health, and require attention.

The Construct allows conceptualisation of IMS into generic functional elements, which can go through the process of coding. The IMS Construct allows retaining most of the generic

characteristics of a particular task or process at the higher levels of the software. IMS functionality specific to power and battery monitoring scenarios rises from User-defined adaptation of the generic Construct. In this respect, the IMS software is not hardware specific, and hardware devices different from the hardware described herein could be used. Specific coding to interface the IMS hardware to the IMS software occurs at low levels and does not involve higher level processes.

There are seven Primary Elements (PE) of the IMS Software Construct, and these are illustrated in block diagram form in Figure 19. The purpose of each of the Primary Elements is described briefly below.

Primary Element	Description
Configuration and Security (CS)	This procedure allows the Owner to define the operational functions of the IMS. Birth (initialisation) occurs through the configuration modules via the serial port only. Birth creates the Primary Task list for the Sequencer. The Owner-User Security monitor is located in this element. Wake-up (after power down instances) or re-configuration by the Owner also is vectored through this element. Limited self-testing is performed during configuration before passing control to the Primary Sequencer.
Primary sequencer (PS)	This is the high level process engine which polls through the task list. The task list originates from the Configuration Element. This process assembles and passes time-based requests for activity by one or more of the other Primary Elements.
User Interface (UI)	This element handles all User-interface interaction and data transfer. This includes all keypad and LCD display processes and all digital communications via the serial port.
Analysis (expert-system) Engine (AE)	This process is a high level background task which performs all data checking, exception condition testing and trend estimates, according to Owner-defined options at configuration time. The event recorder functions are also embedded in this process.
Database Engine (DBE)	This is a mid-level process which takes the current real-time data and performs the second level data averaging and statistical manipulation (as defined by the Owner at configuration time). This process also builds the binning scheme used in the trend recording.
User-defined Reality Translator (RT)	This process takes and manipulates raw sampled data from actual input channels and derives a virtual-inputs matrix. A virtual input is a real physical input or the mathematical or temporal combination of one or more physical inputs. The virtual inputs are then associated with parameters, units and scaling defined by the User, prior to feeding the Database.
Analog Input Engine (AIE)	This is the core, or inner-most process. This process assembles the time-dependent input channel sampling matrix and acquires real-time data accordingly. Auto-ranging and first level data averaging is done in this process.

Figure 18 is a block diagram which illustrates the general input processing structure of the IMS. The physical inputs 302 are, in use, each coupled to a node in the power system to be monitored, or to a transducer or measuring apparatus such as a temperature sensor or the like

for measuring a related quantity. Each of the physical inputs is identical and so may be arbitrarily coupled to the nodes to be monitored, and it is the connectivity matrix 340 which stores a correspondence between the physical inputs 302 and the monitored system nodes. The software controls a multiplexer matrix (described in greater detail hereinbelow) based on the connectivity matrix 340 in order to provide appropriate connections to measure desired electrical potential differences between various ones of the monitored system nodes. Thus, the connectivity matrix 340 contains the information which links otherwise arbitrary physical inputs with particular electrical quantities which are desired to be monitored by the IMS.

The combinations of physical inputs 302 which are dictated by the connectivity matrix 340 define a set of measured parameters 350 which represent the potential differences between various nodes in the monitored system, or other voltage based measurements representing quantities such as impedance and temperature. An association data matrix 360 is constructed to allow the measured parameters 350 to be assigned a correspondence to a set of virtual parameters 370. Each of the virtual parameters 370 incorporates any scaling factors which may be required in order to make the monitored measurements meaningful, and each virtual parameter is associated with a unit of measurement corresponding to the measured quantity (e.g. volts, milliamps, ohms, etc.). In the simplest case a virtual parameter may correspond directly to a pair of physical inputs between which a potential difference is measured. However the virtual parameters are not limited to a direct correspondence with the physical inputs 302 or measured parameters 350, and the association matrix 360 may define virtual parameters which are combinations of other defined virtual parameters. For example, a virtual parameter representing an electrical power measurement can be defined in the association matrix as a multiplication of a first virtual parameter representing a voltage measurement and a second virtual parameter representing a corresponding electrical current measurement.

Once the virtual parameters have been established, the monitored values are sampled and stored in a data storage memory 380 at selected time intervals. The sampling and storage rates need not be the same. The structure of the data storage memory and the storage procedure employed is described in greater detail hereinbelow.

Input Associations
• Battery bank(s) voltage and impedance • Cell or Monoblock voltages and impedances • Interconnection voltages and impedances • String float and load current • System temperatures • Amp-hours passed • Array current input (solar)

Table 3: List of typical system parameters measured and utilised in the IMS

A functional block diagram of a preferred embodiment of the IMS 2 is shown in Figure 1. The IMS 2 comprises generally a digital processing circuit 100, a power supply circuit 200, an analog processing circuit 300, and an impedance measurement circuit 400. The IMS 2 illustrated is adapted for monitoring a battery stand-by power system, such as in a telecommunications exchange or the like, and the purpose of the impedance measurement circuit 400 is for impedance measurement of lead-acid batteries. Accordingly, in a monitoring system which does not utilise lead acid batteries the impedance measurement circuit 400 may not be required, although other impedance measurements may be advantageous in other applications of the IMS.

A plurality of analog voltage inputs 303 from the monitored apparatus are provided to the IMS 2 by way of an analog I/O connection 302. The analog voltage inputs 303 pass from the analog I/O connection 302 to an input multiplexer matrix 40 of the analog processing circuit 300. Selected signals from the input multiplexer matrix 40 are passed to an input gain and attenuation stage 44 which provides an auto ranging function. From the input gain and attenuation stage the signals are passed to an analog to digital conversion stage 64 whereat the signals are converted to digital representations for processing by the digital processing circuit 100.

The digital processing circuit 100 comprises a general purpose central processing unit having, for example, a microprocessor, memory in the form of RAM and/or ROM, and input/output

interface devices such as a keypad and LCD display. The digital processing circuit 100 also includes digital interface ports enabling digital signals to be received from the analog processing circuit 300 and control signals to be issued to the impedance measurement circuit 400 and analog processing circuit 300. A serial port (not shown) is also provided to enable digital communications with circuitry external to the IMS 2.

The power supply 200 receives its primary power from an external system via line 202 and provides the appropriate voltage level power for the analog processing circuit 300, the digital processing circuit 100 and the impedance measurement circuit 400, and preferably derives this power from the monitored system. The power supply 200 is in the form of a wide range switch mode power supply, which enables it to be supplied with input voltages in a wide range (eg 8 volts to 100 volts) whilst still providing a regulated output suitable for the processing circuits of the IMS 2.

The impedance measurement circuit 400 is provided, as mentioned, for measuring the impedance of batteries, for example, in the monitored power system. The impedance measurement circuit 400 operates by injecting an alternating current into the battery to be measured via an I/O connection 402, along with synchronous detection of the voltage thereat. The impedance measurement circuit 400 may comprise a system, for example, of the type described in the specification of Australian Patent No. 688298, the disclosure of which is incorporated herein by reference. Other impedance measurement techniques may alternatively be employed, of course.

Figures 2 to 12 constitute a component level circuit diagram of the IMS 2. Briefly, Figures 2 to 5 and 12 comprise circuit diagrams representing the digital processing circuit 100, Figures 6 and 7 illustrate the analog processing circuit 300, Figure 8 illustrates the switch mode power supply 200, and Figures 9, 10 and 11 illustrate the impedance measurement circuit 400.

Referring firstly to Figures 2 to 5 and 12, the illustrated form of the digital processing circuit

100 comprises a single chip micro controller 10, which is coupled to a programmable peripheral device 12. The micro controller 10 and programmable peripheral device 12 are coupled together in conventional manner by way of address and data buses. The programmable peripheral device 12 provides additional decoded interface lines on ports A (shown as PAØ to PA7) and B (shown as PBØ to PB7) for controlling the analog processing circuit 300 and impedance measurement circuit 400, as well as other portions of the digital processing circuit itself. A memory circuit 14 is coupled to the address and data buses and control lines from the programmable peripheral device 12, and in this instance comprises a one Mbit RAM (128 kbytes) with SmartWatch DS1216D (Figure 3). An LCD display I/O port 16 is also connected to the data bus and control bus for interface to an LCD display device, and a keypad encoder 18 interconnects the databus with a keypad 20, of conventional form.

Referring to Figure 5, the lower address bus 11 is provided as input to a gate array logic circuit (GAL) 30 which decodes addresses into a plurality of control lines for controlling the analog processing circuit 300. The GAL 30 also provides a clocking input to a gate array logic circuit 32 which receives the databus 13 as input for decoding to control lines RD0 to RD7. An octal latch 34 is also clocked by an output of the GAL 30, and latches the databus 13 to respective inputs of driving transistors 36 which drive control lines RS0 to RS7. The control lines RD0 to RD7 and RS0 to RS7 constitute the control lines for the input multiplexor matrix 40 described hereinbelow.

Interface circuitry 22 and communications circuitry 120 (Figures 4 and 12, respectively) provide the capability for additional communication with the digital processing circuit 100. Interface circuitry 22 enables access to CPU ports A and D (shown as PDØ to PD5), and interfaces serial transmit and receive lines (TXD, RXD) between the micro controller 10 and communications circuit 120. The transmit and receive lines are coupled through opto-couplers 126 to an RS232 line generator 122, which provides an RS232 port for serial communication with the digital processing circuit 100.

The control lines RD0 to RD7 and RS0 to RS7 are coupled from the logic and latching

circuitry of the digital processing circuit 100 (Figure 5) to a multiplexor matrix array 40 (Figure 6), which comprises a plurality of photo-MOS relays 42. 64 voltage inputs from the monitored apparatus are provided to the IMS by way of the analog I/O connection 302, and the analog voltage inputs are coupled to respective photo-MOS relays 42. The photo-MOS relays are arranged in a matrix configuration and controlled by the aforementioned control lines RD0 to RD7 and RS0 to RS7, in order to multiplex the 64 analog voltage input lines onto 2 analog voltage output lines (A and B). The analog output lines A, B from the MUX array 40 are coupled to additional multiplexing circuitry 45, in the form of photo-MOS relays 46, 48 and 50, shown in Figure 7. The multiplexing circuitry 45 is controlled by control line V/Z from the digital processing circuit 100, and allows inputs B_0, B_1, A_0 and A_1 from the impedance measurement circuit to be multiplexed with the voltage lines A , B. The outputs A', B' from the MUX circuit 45 are applied across series resistors R12, R13, R14, R15, R16, R17, R18 and R19 which constitute a voltage divider 52. Outputs of the voltage divider 52 are coupled to a further multiplexing circuit 54 comprising photo-MOS relays 56, 58 which are controlled by control lines ATT0 to ATT3 provided from the GAL circuit 30 (Figure 5). The voltage divider 52 and MUX circuit 54 provide the auto ranging function of the analog processing circuit 300. Appropriate application of the control lines ATT0 to ATT3 enables an output of the voltage divider 52 (Figure 7) to be selected which provides an output on lines HI, LO, which is in a range (eg -5 volts to +5 volts) which is suitable for digital processing, as long as the input analog voltage does not exceed the maximum input voltage limit. The appropriately attenuated analog signal on lines HI, LO are provided as input to a precision instrumentation amplifier circuit 60. The amplifier circuit 60 allows amplification of the analog signal in the event that this is required, and the amplification is controlled by control line GAIN from GAL circuit 30, switched through photo-MOS relay 62. The output of amplifier 60 is coupled to the analog input of an analog to digital converter circuit 64 (having 12 bits of magnitude resolution plus one bit of sign data), for conversion of the analog voltage signal level to a digital representation which is output on the databus 13. A precision 12 volt reference circuit 66 provides a reference voltage input to the A-D convertor 64.

The wide range switch mode power supply 200 is illustrated in component form in Figure 8,

and details of its operation are omitted here so as to prevent obscuring the clarity of description of the invention as a whole. Briefly, input power is provided at V_x and V_y, and is rectified and regulated through voltage regulators 76 to provide supply voltages of ± 5 volts at V_d and V_s and ± 12 volts at V_{dd} and V_{ss}. The power supply 200 is able to operate on input voltages between about 8 volts and 100 volts, and this wide range is facilitated by the use of a pulse width modulation (PWM) controller 72 and voltage reference diode 74 which is coupled thereto by way of an opto-coupler 75. The detailed operation of the switch mode power supply 200 will be readily ascertainable by those skilled in the art from the circuit level diagram provided in Figure 8.

Figures 9, 10 and 11 illustrate the circuitry for the impedance measurement circuit 400. A single frequency current injection circuit 80 is illustrated in Figure 9, and the operation will be readily apparent to those skilled in the art from a detailed examination of the circuit in conjunction with the theory of operation of such a battery impedance measurement circuit as described in the aforementioned Australian patent specification. In essence, a single frequency signal is generated by a frequency generator 82, is amplified using power darlington transistors 84, and output on lines -I, +I. The current injection signals -I, +I are provided to an array of reed relays 116 (Figure 11) which form part of a switching circuit 110 controlled by a programmable gate array logic circuit 114. The GAL 114 is driven from the databus 13, and enables the current injection signals to be selectively output through output connector 115 to battery terminals of the monitored apparatus. The impedance receiving and demodulating circuitry for impedance measurement circuit 400 is shown in Figure 10, which is provided with an AC input voltage signal on lines INA and INB. The input signals are amplified through an instrumentation amplifier 92, and demodulated using a synchronous demodulator circuit 94 and output through a low pass filter 96.

Impedance measurements which are taken in this way can vary depending upon the actual length of the electrical cables which are used to couple the IMS physical inputs to the nodes of the monitored system. In order to alleviate this difficulty the IMS may be arranged with a dedicated input channel to which is coupled an accurately known electrical resistance. By

taking an impedance measurement across the known resistance, including whatever connecting leads are used, and comparing the measured value with the known resistance value the IMS controlling software is then able to determine a calibration constant for impedance measurements, which may then be factored in to the monitored impedance values before storage thereof. For example, the calibration factor may be included in the association matrix 360 during calculation of the virtual parameters 370 (Figure 18). In practice it has been found suitable to in fact provide two known impedances, one which is situated on board as part of the IMS circuitry and the other which is coupled to the input circuitry of the IMS by way of leads corresponding to the longest used for coupling other monitored nodes to the IMS. By taking one measurement from the on-board impedance and another from the known impedance and leads, the IMS controlling software is able to determine a linear correction factor for impedance measurements which then take into account the resistance added by the connecting leads, thus enabling more accurate impedance measurements to be taken.

Figure 13 shows a block diagram of the analog processing circuit 300, for the purposes of simplified explanation. Sixty-four analog voltage inputs are provided to the input multiplexor matrix 40 through analog I/O connection 302. The MUX 40 is in the form of a matrix of photo-MOS relays 42 (Figure 6), which are utilised as the switching elements because of their ability to handle up to about 2000 volts at the controlled input without breakdown. Furthermore, the photo-MOS relays do not use as much power as, for example, mechanical relays, which is important where the IMS is to be powered from the monitored apparatus such as a battery stand-by power system. Sixteen control lines RS0 to RS7 and RD0 to RD7 are also provided as input to the MUX array 40. One of each of RS0-7 and RD0-7 are active at any given time, so as to select 2 of the 64 analog inputs to be passed through the MUX 40 to outputs A, B. The analog voltage provided at the selected output lines A, B is applied across a voltage divider circuit 52, which comprises a plurality of series connected resistors (see Figure 7). Taps on the voltage divider 52 provide a plurality of voltage signal outputs having respective voltage magnitudes of some fraction of the potential difference between output lines A and B. The respective fractional voltage outputs are provided to multiplexing selection circuit 54, at which one of the fractional voltage outputs is selected according to control lines

ATT0 to ATT3. The fractional voltage output is selected according to which one has a voltage level most appropriate for digital signal processing. For example, if the analog voltage input is quite large (eg of the order of 100 volts) then the fractional voltage output which would be selected would be that having the greatest attenuation so that the fractional voltage output is of the order of 5 volts. On the other hand, if the analog voltage input is quite small (of the order of 4 volts), then the fractional voltage output selected may be that output having no attenuation.

As mentioned, the output from the voltage divider 52 having the appropriate amount of attenuation is selected by use of the control lines ATT0 to ATT3 through the multiplexor selector 54. The control lines ATT0 to ATT3 are controlled from the digital processing circuit 100, and may be controlled according to a predetermined selection criteria corresponding to the active control lines to the input multiplexor matrix 40. For example, the digital processing circuit may be pre-programmed to activate a particular one of the control lines ATT0 to ATT3 for each selection of the MUX circuit 40 on the basis of a priori knowledge of the expected analog voltage signal amplitude for the MUX 40 selection. Alternatively, a feedback arrangement from the output of the multiplexor selector 54 may be provided to the digital processing circuit 100, including at least one voltage comparator, comparing the output of the MUX 54 with a reference voltage to determine which selection of the MUX 54 provides an output in a suitable range for processing by the analog to digital convertor 64. In practice it has been found suitable to begin each measurement with the voltage divider on the highest possible attenuation, and cascade successively through the attenuation levels until the attenuated input signal is in the appropriate range, which may be judged by way of the overflow register of the analog to digital converter.

The output from multiplexor selector 54 is passed to an amplifier section 60, which is provided to boost the signal amplitude of analog input signal levels which are too low for good conversion to digital quantities. In the case of such an input signal with low amplitude, whether it be known a priori or detected using a level comparator as discussed above, the signal selected from the voltage divider 52 by the MUX 54 is without attenuation, and a

GAIN signal is applied to the amplifier 60 in order to boost the output amplitude thereof. The GAIN signal is similarly provided from the digital processing circuit 100. In the case of a signal which has been attenuated by the voltage divider 52 the gain control may or may not be applied, depending upon the actual signal amplitude required.

The output of amplifier 60 is coupled to the input of an analog to digital conversion circuit 64 which, in the case of the preferred embodiment, converts the analog input to a 12 bit digital representation thereof. The digitally converted signal is output onto the databus 13 for processing and/or storage by the digital processing circuit 100.

The flow chart 150 shown in Figure 14 illustrates the basic procedure carried out by the IMS apparatus. The first step (step 152) is the selection of an analog input from the plurality of analog voltage inputs at the analog I/O connection 302. This is performed by the input multiplexor matrix circuit 40, and may entail selecting a pair of inputs from 32 pairs, for example. The analog voltage inputs are provided from sources external to the IMS apparatus, and may include direct voltage readings from various parts of the power system, for example, together with other forms of voltage inputs from sensors such as temperature sensors, current sensors and the like. Analog voltage signals from the impedance measurement circuit 400 are considered in this category also, although the impedance measurement circuit 400 itself forms part of the IMS in the preferred embodiment. Once a particular analog input has been selected, scaling of the analog signal must be adjusted utilising an auto ranging circuit (step 154). This is required to enable the IMS to receive analog inputs within a broad range of signal levels which facilitates flexibility of the IMS apparatus. For example, in the preferred embodiment, analog signal levels within the range of -160 to +160 volts can be handled. Because of the wide range of possible analog input voltage levels, it is necessary to adjust the scaling according to the particular selected analog input before conversion to digital representation, since an analog to digital convertor circuit can typically only handle voltages within a much smaller range. For example, an A/D convertor may be adapted to convert analog signals which are only in the range of -5 to +5 volts, and input voltage levels outside that range may damage the circuit, or at least saturate the output. Although it would be

possible to simply attenuate all of the analog input signals the same amount so that the maximum input voltage level corresponds to the maximum voltage level presented to the A/D convertor, this would necessarily reduce the accuracy of measurement samples for input signals having levels significantly less than the maximum. It may also be necessary to provide for amplification of some analog input signal levels for the same reason, and for this purpose the aforementioned amplifier circuit 60 is provided.

Once the scaling of the analog input signal level has been adjusted to an appropriate range for the A/D convertor (64), the signal is repeatedly sampled over a time slice period of, for example, several milliseconds, at step 156. The actual number of samples taken may depend upon the time slice period which is selected, which may in turn depend upon the actual number of analog inputs to the multiplexing circuit 40 and the frequency with which it is desired to determine the level of each input. For example, if there are 32 analog inputs and it is desired to determine the signal level of each input once every second, then it would be possible to set each sampling time slice period to approximately 30 milliseconds. The number of samples of a particular input which can be taken during the time slice period will of course depend upon the sampling speed of the A/D convertor. The repeated sampling of an analog input over a time slice period enables transient fluctuations which are shorter in duration than the time slice period to be averaged out. In order to deal with these fluctuations, the plurality of samples taken during the time slice period are averaged over the time slice in step 158 and stored in a sampled data pool in the digital processing circuit 100. The next analog input is then selected using the multiplexing circuit 40 (step 160), before the procedure returns to step 154 to adjust the scaling for the new analog input voltage level. Transient fluctuations could alternatively be accommodated by using a sample-hold technique in the analog-to-digital conversion process.

In the above mentioned example where the level of each analog input is determined once every second, it is immediately apparent that, in the context of a monitoring system, the amount of memory which would be required in order to store every averaged sample for every input over any substantial length of time would be quite large. For example, in that scenario

approximately 20 megabytes of memory would be required in order to store one weeks worth of sampled data. Clearly this is prohibitive for a monitoring system which may be required to operate unattended over lengths of time of the order of years. Accordingly, the IMS apparatus of the preferred embodiment implements a "bin storage" system for storing sampled analog input data over a long period of time, and at the same time providing a useful representation of that data over various time frames. This storage procedure is represented by step 162 in flow chart 150, and is illustrated in greater detail in flow chart 170 shown in Figure 15.

The flow chart 170 shown in Figure 15 illustrates the "bin storage" procedure for storage of sampled data in the digital processing circuit 100 of the IMS 2. The analog voltage inputs are provided at stage 172, and time based data acquisition of the analog input voltage levels are obtained at stage 174. The time based data acquisition stage 174 in this case includes both the multiplexing by use of MUX 40 under control of the digital processing circuit, and the repeated sampling over a time slice period discussed hereinabove in connection with Figure 14. The plurality of instantaneous values 175 for each input channel which are obtained from stage 174 are averaged for each channel at stage 176 in order to reduce the effect of fluctuations and the like which are shorter in duration than the time slice period. The averaged point values 177 for each channel, generated at stage 176, are passed to the sampled data pool 178 and stored for a predetermined time in, for example, a circular memory or FIFO buffer. From the sampled data pool 178 the averaged sample data is then processed into the bin storage memory at stages 180 to 194, as described hereinbelow.

The bin storage process involves a sequence of averaging engines and loop memories. Each loop memory stores data over a different length of time, and during that length of time the data therein is averaged and stored in the next loop memory having a longer term. In the example shown in Figure 15, the bin storage includes a short term loop memory 182 which holds 8 hours worth of data, with each data element representing a 5 minute interval of the input signals monitored by the IMS. Thus, advantageously the sampled data pool 178 is arranged to store at least 5 minutes worth of averaged sample data which, as mentioned, may

be taken at 1 second intervals. For each channel, the short term averaging engine 180 takes the most recent 5 minutes worth of 1 second interval averaged sample data (eg 300 averaged samples) and applies an averaging algorithm to reduce the stored averaged sample data for that channel to a single short term data element. The short term averaging engine 180 and the short term loop memory 182 form part of the short term trend 181, which is used for analysing changes in system parameters over the short term.

While an averaging engine is utilised for stage 180 (and for stages 184, 188 and 192, discussed below), the algorithm carried out thereby may not in fact comprise an averaging process in the traditional sense, and several different techniques may be advantageously employed. For example, instead of merely summing the data samples and dividing by the number of samples, as in a traditional averaging process, the averaging engine 180 (184, 188, 192) may alternatively apply a threshold, for example, to determine how often the sampled data value rises above or falls below a given threshold. Other common processing techniques may alternatively be applied, and will be apparent to those skilled in the art.

In any event, the processing applied by the short term averaging engine 180 reduces the 5 minutes worth of sampled data in the sampled data pool 178, for each channel, to a single short term data element which is stored in the short term loop memory 182. Over an eight hour period this data element passes from the input to the output of the short term loop memory 182 which, when full, comprises 96 data elements for each channel, each representing a 5 minute interval.

Once each hour the most recent 12 data elements in the short term loop memory 182 are examined by the mid term averaging engine 184. These 12 data points are averaged using the same process as the short term averaging engine 180, although a different process may alternatively be applicable. The result from the mid term averaging engine 184, for each channel, is a mid term data element each hour, representing one hour of sampled data for each channel respectively. The mid term data element is provided, as to the input of a mid term loop memory 186, which has a capacity of 192 one hour data elements for each channel,

representing an 8 day history for each channel. The mid term trend 185 is similar to the short term trend 181 but except that the analysis is carried out over longer sampling intervals.

Similarly, a long term averaging engine 188 samples the most recent 24 mid term data elements in the mid term loop memory 186 once per day. The output of the long term averaging engine 188 is provided to the input of a long term loop memory 190 and is used in the long term trend 189. The long term loop memory ideally has a capacity of 90 one day interval long term data elements for each channel. Finally, once every 30 days the most recent 30 long term data elements are averaged by a history building engine 192, and stored in a history register memory 194, which retains one month averaged data for each channel for the life of the monitoring installation of the IMS.

The bin storage process is particularly useful in that it provides an indication of a trend in sampled data for each channel over a plurality of time frames. Furthermore, depending upon the algorithm utilised by each averaging engine 180, 184, 188, 192, relevant events in the monitored parameters represented by the sampled channels will be preserved, and trends in the behaviour of the parameters can be observed over the time frames represented by the various loop memories of the bin storage system. The history register preserves the behaviour of the monitored parameters over the lifetime of the IMS installation, the long term loop memory stores the most recent 90 days of behavioural data at one day resolution, the mid term loop memory stores the most recent 8 days of parameter data of 1 hour resolution, the short term loop memory continually holds the most recent 8 hours of parameter data of 5 minute intervals, and the sampled data pool at any time holds 5 minutes worth of parameter data for each input channel at the finest resolution of 1 second intervals.

The form of the data provided by the bin storage process is advantageous not only for analysis of past performance of the monitored apparatus, but can also be useful for predicting future performance. As mentioned, the bin storage provides, in the described example, data which can indicate trends in the monitored apparatus parameters over a plurality of time frames, and these trends can be utilised in some instances to predict future performance of the monitored

parameters. For example, in a typical application of the IMS in which the impedance measurement circuit 400 is employed to measure the impedance of battery cells in a standby power system, these impedance measurements are presented to the analog processing circuit 300 amongst the other analog input signals. Because the impedance measurements are made very frequently by the continuously monitoring IMS, the resulting impedance (Z) measurement data is of very high resolution and wide dynamic range. Taken over a time period such as that stored in one of the loop memories of the bin storage system, the IMS allows measurements of the differential of battery impedance to be calculated (dZ/dt). The battery impedance differential (dZ/dt) can in fact be utilised as a predictor of battery performance, and is particularly useful where a plurality of batteries can be compared against one another, as is the case in, for example, a telecommunications exchange standby battery power system. The IMS can measure dZ/dt for all batteries, or all cells, in a bank of batteries of the power system and, over a period of time for the data stored in the bin storage, determine which battery will be the first to fail. This is due to the performance of lead acid batteries in which it has been generally shown that of a plurality of batteries, that with the highest dZ/dt at any given time will be the battery to fail first of those plurality of batteries. This function can be achieved with the continuous monitoring and bin storage system of the IMS, but has been unfeasible in traditional battery measurement systems. In conjunction with other measured information as gathered and analysed by the expert system in IMS, the battery impedance time differential can be used as the basis of a run-time predictor during discharge.

As discussed hereinabove, the controlling software of the IMS is based on an owner-user model, and at the time of manufacture or installation certain parameters and settings of the IMS are required to be initialised by the "owner". These settings include details of the connectivity matrix 340 to instruct the controlling software in the selection of appropriate physical inputs for each desired measured parameter 350, and details of the association matrix 360 for determining the desired virtual parameters 370 from the measured parameters. The association matrix 360 will preferably also include stored indications of any desired scaling factors and units applicable to the virtual parameters. The owner is also responsible for initialising the data storage memory (the "bin memory") and the storage configuration

parameters associated therewith, such as the measurement sampling rate and data storage interval for each of the averaging engines. Only the owner is entitled to reset the data storage memory to discard any saved data, but the stored data is not able to be edited - even by the owner. The configuration of the IMS can be changed by the owner using commands sent to the digital processing circuit 100 by way of the communications circuit 120 (Figure 12). Further, a plurality of IMS devices can be daisy-chained, even between different sites, so that the owner can broadcast configuration changes to multiple IMS controllers at once.

The user, on the other hand, has only limited access to the functions of the IMS. The main concern of the user is to be able to obtain access to the data stored in the IMS during monitoring, and this can be done on site or remotely through the communications circuitry 120. The user is not able to edit or erase the stored data. Certain exception conditions used by the IMS to determine when to raise an alarm or the like may be set or altered by the user, primarily those conditions which require to be varied from time to time depending upon prevailing conditions in the monitored system.

In the event that the IMS detects a change of environment, such as by disconnection from it's source of power or the like, when the IMS is powered up once again the controlling software changes the mode of operation. If a change of environment is detected the controller can no longer be certain that the configuration settings with which it has been programmed by the owner are applicable to the new environment, and thus to avoid the possibility of incurring any damage the IMS reverts to a "dumb" operation mode. In this mode the virtual parameter configurations programmed by the owner are ignored, and the IMS essentially reverts to a multiplexed voltmeter in which voltage levels are measured at each of the physical inputs at predetermined intervals, for example 1 second intervals. The binning memory procedure is not implemented and the measured voltage levels are merely stored as raw data in the memory. The IMS software does, however, allow the Owner or user to accommodate situations where only some component elements of the system being monitored are physically removed or changed in time (for example, replacement of a single battery cell) without loss of previously stored information about other elements of the system which are not changed.

The foregoing detailed description of the present invention has been presented by way of example only, and is not intended to be considered limiting to the invention which includes every novel feature and novel combination of features herein disclosed.

Throughout this specification and the claims which follow, unless the context requires otherwise, the word "comprise", and variations such as "comprises" and "comprising", will be understood to imply the inclusion of a stated integer or step or group of integers or steps but not the exclusion of any other integer or step or group of integers or steps.

CLAIMS:

1. A monitoring system for monitoring parameters of an apparatus, comprising:

a plurality of inputs for receiving a plurality of electrical analog signals representative of parameters of said apparatus;

a multiplexing circuit for multiplexing said analog signals into sequential analog input signals;

an auto-ranging circuit for individually scaling each of said sequential analog input signals to within a predetermined range suitable for digital processing thereof;

a signal converter for converting the scaled sequential analog input signals into respective digital signals; and

digital processing means for storing and/or manipulating said digital signals.

2. A system as claimed in claim 1 wherein said multiplexing circuit comprises an array of photo-MOS elements.

3. A system as claimed in claim 2 wherein said photo-MOS elements are controlled by said digital processing means to perform a multiplexing function.

4. A system as claimed in claim 1 wherein said auto-ranging circuit comprises a plurality of auto-ranging photo-MOS elements.

5. A system as claimed in claim 4 wherein said auto-ranging circuit further comprises a plurality of resistive elements across which said sequential analog input signals are selectively applied by said auto-ranging photo-MOS elements.

6. A system as claimed in claim 5 wherein said plurality of resistive elements are used to provide voltages of selected proportions of one of said sequential analog input signals to said auto-ranging circuit, wherein respective said auto-ranging photo-MOS elements are coupled to one or more of said plurality of resistive elements to selectively generate an output

within said predetermined range.

7. A system as claimed in claim 6 wherein said auto-ranging circuit comprises an analog signal amplifier circuit for increasing a voltage level of one of said sequential analog input signals to within said predetermined range.

8. A system as claimed in claim 7 wherein said auto-ranging circuit comprises a sample-and-hold circuit for smoothing changes in the respective magnitudes of said sequential analog input signals.

9. A system as claimed in claim 1 wherein the monitoring system is powered by a wide range switch-mode power supply.

10. A system as claimed in claim 1 wherein the monitoring system may be powered by a system which said monitoring system monitors.

11. A system as claimed in claim 9 wherein said power supply is adapted to automatically adjust to differing input voltage sources.

12. A system as claimed in claim 1, further including impedance measuring means for measuring the impedance of a circuit of said apparatus.

13. A method for monitoring parameters of an apparatus, comprising the steps of:

receiving a plurality of electrical analog signals representative of parameters of said apparatus;

multiplexing said analog signals into sequential analog input signals;

scaling each of said sequential analog input signals to within a predetermined range suitable for digital processing thereof;

converting the scaled sequential analog input signals into respective digital signals using signal converter means; and

storing and/or manipulating said digital signals using digital processing means.

14. A method as claimed in claim 13 wherein said digital signals are representative of data sampled over a first time interval, and said step of storing and/or manipulating includes averaging a plurality of said digital signals over said first time interval to produce a first averaged data value.

15. A method as claimed in claim 14 wherein said step of storing and/or manipulating further includes averaging a plurality of said first averaged data values over a second time interval to produce a second averaged data value.

16. A method as claimed in claim 15 wherein said step of storing and/or manipulating further includes averaging a plurality of said second averaged data values over a third time interval to produce a third averaged data value.

17. A method as claimed in claim 16 wherein said step of storing and/or manipulating further includes averaging a plurality of said third averaged data values over a fourth time interval to produce a fourth averaged data value.

18. A method as claimed in claim 17, further including the step of storing a plurality of said first, second, third or fourth averaged data values in respective memory means.

19. A method as claimed in claim 13 wherein said step of multiplexing is performed by a multiplexing circuit comprising an array of photo-MOS elements.

20. A method as claimed in claim 19 wherein said photo-MOS elements are controlled by said digital processing means to perform said step of multiplexing.

21. A method as claimed in claim 13 wherein said step of scaling is performed by an auto-ranging circuit comprising a plurality of auto-ranging photo-MOS elements.

22. A method as claimed in claim 21 wherein said auto-ranging circuit further comprises a plurality of resistive elements across which said sequential analog input signals are selectively applied by said auto-ranging photo-MOS elements.

23. A method as claimed in claim 22 wherein said plurality of resistive elements are used to provide voltages of selected proportions of one of said sequential analog input signals to said auto-ranging circuit, wherein respective said auto-ranging photo-MOS elements are coupled to one or more of said plurality of resistive elements to selectively generate an output within said predetermined range.

24. A method as claimed in claim 23 wherein said auto-ranging circuit comprises an analog signal amplifier circuit for increasing a voltage level of one of said sequential analog input signals to within said predetermined range.

25. A method as claimed in claim 24 wherein said auto-ranging circuit comprises a sample-and-hold circuit for smoothing changes in the respective magnitudes of said sequential analog input signals.

26. A method as claimed in claim 13, further including the step of measuring the impedance of a circuit of said apparatus.

27. A monitoring system, comprising:

an input means for receiving at least one electrical signal input;

a data acquisition means for obtaining first data values representing the at least one signal input repeatedly sampled at a first time interval;

a first storage means for storing said first data values;

a first averaging means for generating second data values representing averaged values of said first data values over a second time interval; and

a second storage means for storing said second data values.

28. A system as claimed in claim 27 wherein said monitoring system further includes at least one succeeding averaging means and at least one succeeding storage means, wherein each succeeding averaging means is arranged to generate succeeding data values over a succeeding time interval, representing average values of data values stored in a preceding storage means, and each succeeding storage means is arranged to store said succeeding data values.

29. A system as claimed in claim 27 wherein said second time interval is longer than said first time interval.

30. A system as claimed in claim 28 wherein each succeeding time interval is longer than a preceding time interval.

31. A system as claimed in claim 27 wherein said first and second storage means comprise circular memory means.

32. A system as claimed in claim 27 wherein said first and second storage means comprise a FIFO buffer.

33. A system as claimed in claim 27 wherein the monitoring system is powered by a wide range switch-mode power supply.

34. A system as claimed in claim 27 wherein the monitoring system may be powered by a system which said monitoring system monitors.

35. A system as claimed in claim 33 wherein said power supply is adapted to automatically adjust to differing input voltage sources.

36. A monitor for monitoring a battery, comprising:

battery impedance means for generating sampled impedance measurements of the

impedance of said at least one battery at predetermined sampling intervals; and

storage means for storing digital representations of said sampled impedance measurements in a plurality of memory means, each memory means being adapted to store representations of said sampled impedance measurements generated at respective different time intervals.

37. A monitor as claimed in claim 36 wherein said digital representations are used to generate a measure of a time differential of the impedance of said at least one battery.

38. A monitor as claimed in claim 37 wherein said time differential is a measure of the change in impedance of said at least one battery over time, and said time differential is indicative of a likelihood of failure of said at least one battery.

39. A method of monitoring a plurality of batteries or cells, comprising:

repeatedly measuring an impedance of each of said plurality of batteries or cells over a predetermined time interval;

recording digital representations of the measured impedances; and

determining, using said digital representations, a measure of a time differential of the impedance of each of the plurality of batteries or cells.

40. A method as claimed in claim 39 wherein said time differential is a measure of the change in impedance of one of said batteries or cells over time, and further including the step of predicting, based on a plurality of respective said measures, a likelihood of failure of said battery or cell.

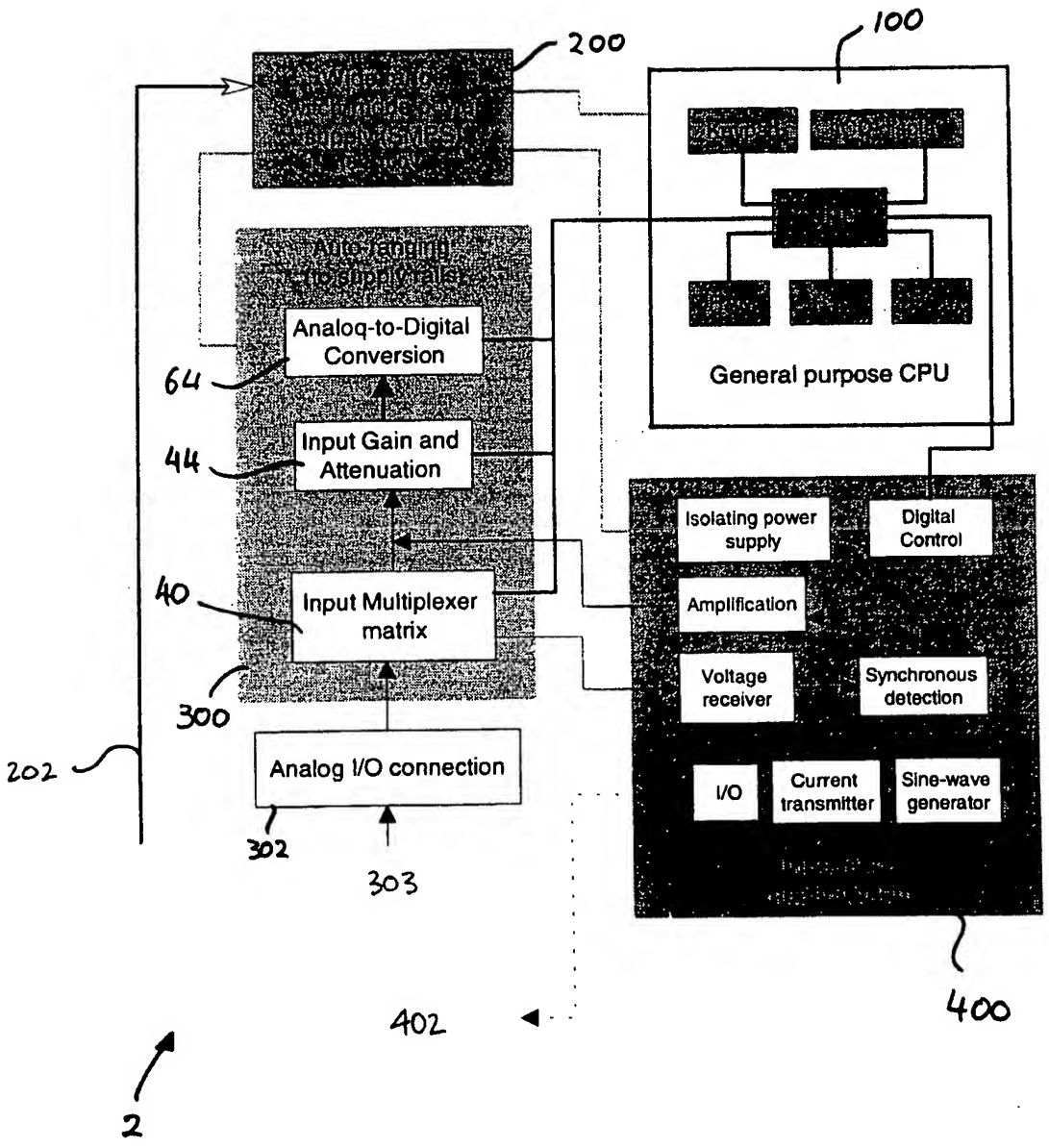
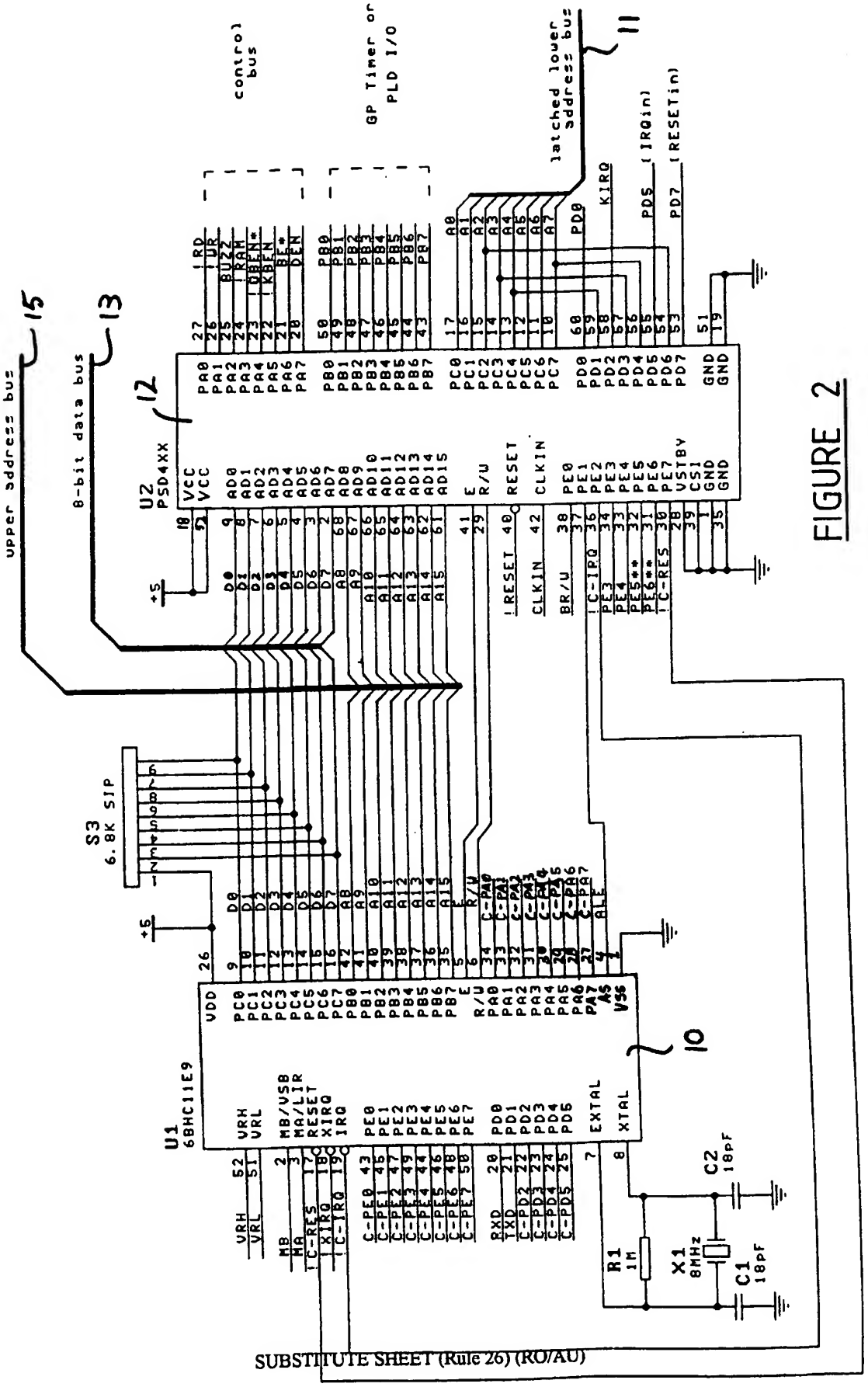

200
100
Auto-ranging to supply rails
Analoq-to-Digital Conversion
64
Input Gain and Attenuation
44
Input Multiplexer matrix
40
300
Analog I/O connection
302
303
202
General purpose CPU
Isolating power supply
Digital Control
Amplification
Voltage receiver
Synchronous detection
I/O
Current transmitter
Sine-wave generator
400
402
2

FIGURE 1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GP Timer or PLD I/O
latched lower address bus
11
upper address bus
15
8-bit data bus
13
12
U2
PSD4XX
U1
68HC11E9
10
S3
6.8K SIP
+5
KIRQ
(IRQin)
(RESETin)
!RESET
CLKIN
R/W
!C-IPQ
!C-RES
VRH
VRL
MB
MA
!C-RES
!XIRQ
!C-IRQ
RXD
TXD
EXTAL
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1M
X1
8MHz
C1
18pF
C2
18pF

FIGURE 2

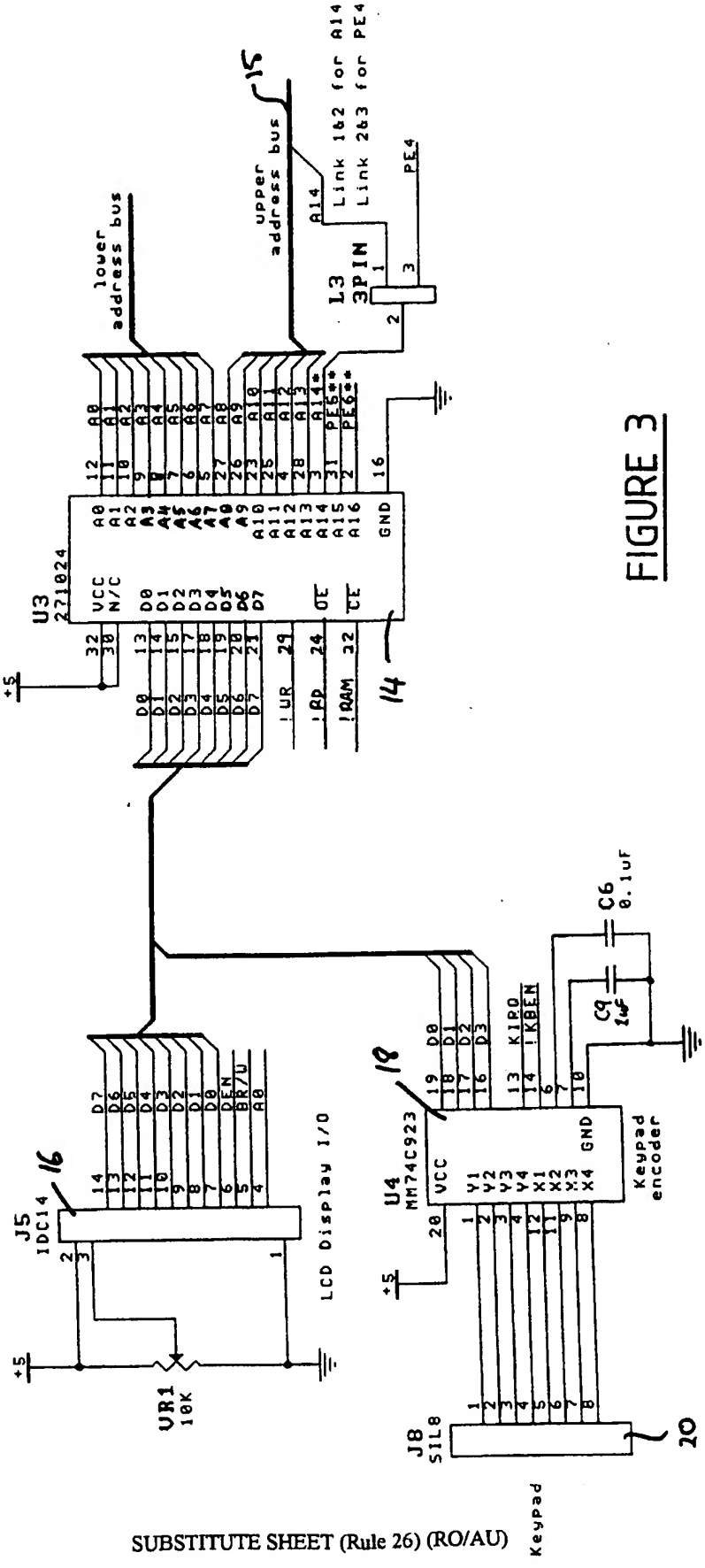

upper address bus
lower address bus
Link 1&2 for A14
Link 2&3 for PE4
L3 3PIN
U3 271024
VCC N/C
GND
OE
CE
!WR
!RD
!RAM
U4 MM74C923
VCC
GND
K1PD
!KBEN
Keypad encoder
C6 0.1uF
C9 1uF
J5 IDC14
LCD Display I/O
VR1 10K
J8 SIL8
Keypad
+5

FIGURE 3

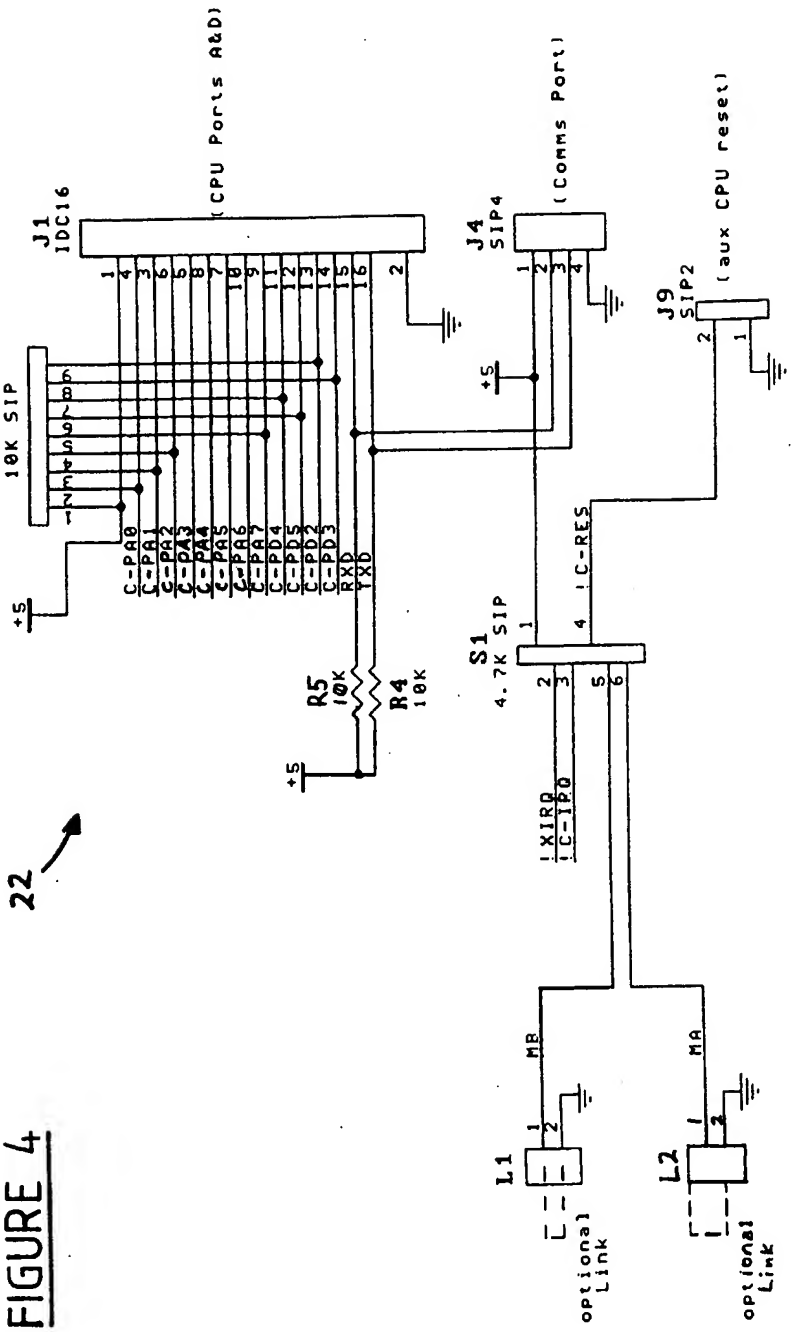

J1
IDC16
(CPU Ports A&D)
J4
SIP4
(Comms Port)
J9
SIP2
(aux CPU reset)
S2
10K SIP
S1
4.7K SIP
R5
10K
R4
10K
+5
C-PA0
C-PA1
C-PA2
C-PA3
C-PA4
C-PA5
C-PA6
C-PA7
C-PD4
C-PD5
C-PD2
C-PD3
RXD
TXD
!C-RES
!XIRQ
!C-IPD
MB
MA
L1
L2
optional Link
optional Link
22

FIGURE 4

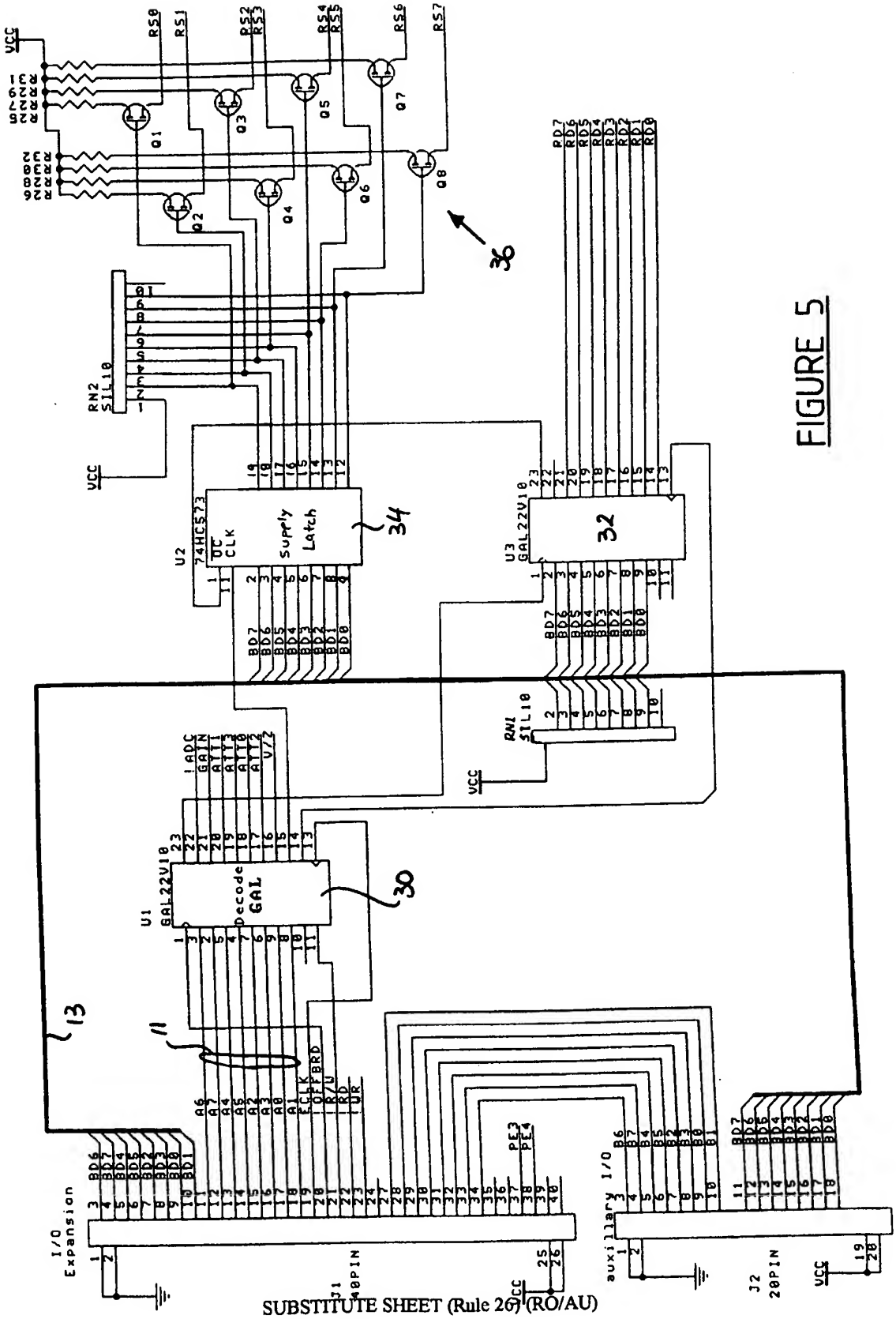

VCC
RS0
RS1
RS2
RS3
RS4
RS5
RS6
RS7
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
36
RN2
SIL10
U2
74HC573
OC
CLK
Supply
Latch
34
U3
GAL22V10
32
RD7
RD6
RD5
RD4
RD3
RD2
RD1
RD0
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
RN1
SIL10
!ADC
GAIN
ATT1
ATT2
ATT3
V72
U1
GAL22V10
Decode
GAL
30
13
11
A6
A7
A4
A5
A2
A3
A0
A1
FCLKFBRD
!R/W
!RD
!WR
PE3
PE4
I/O
Expansion
J1
40PIN
auxiliary I/O
B6
B7
B4
B5
B2
B3
B0
B1
J2
20PIN
VCC

FIGURE 5

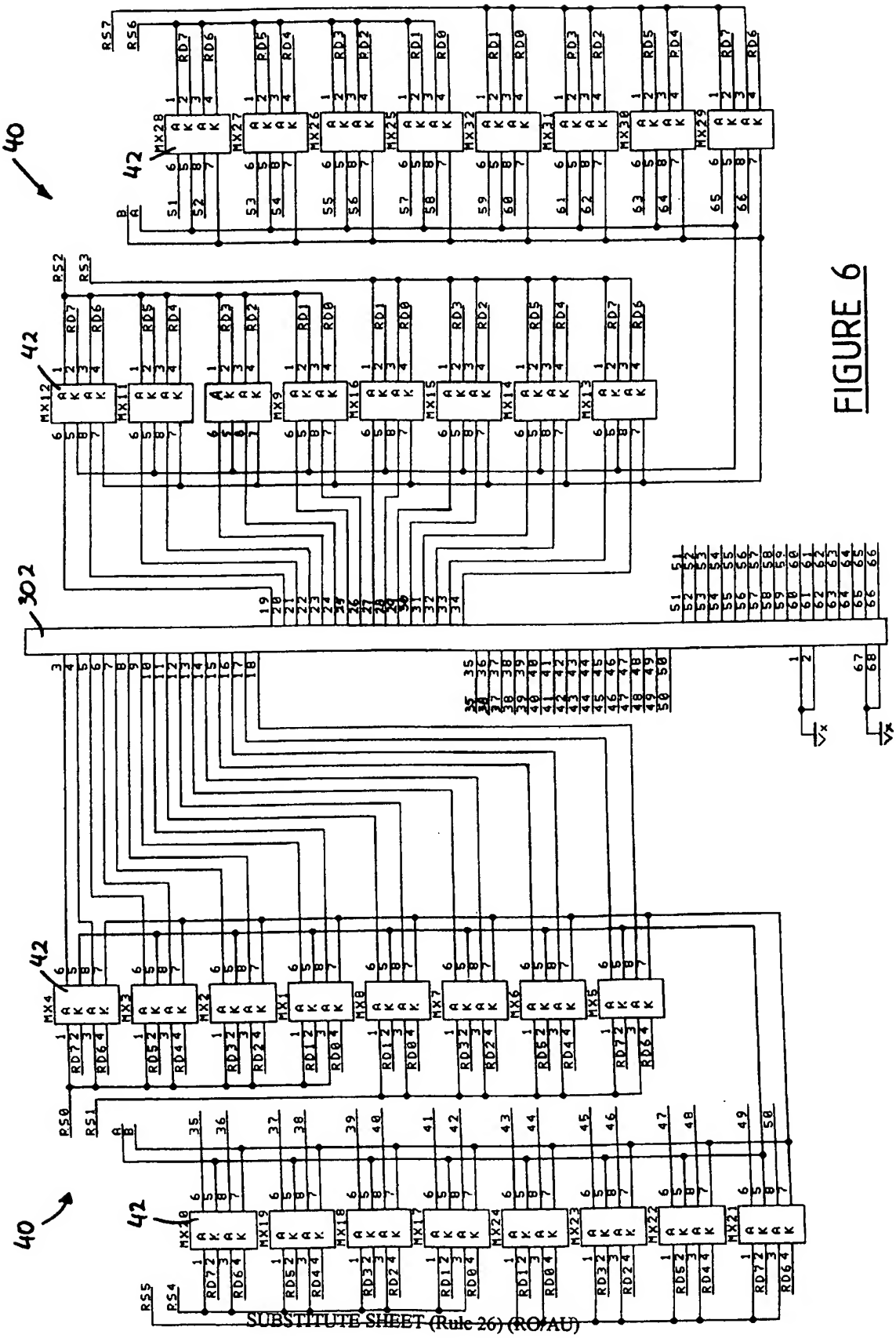


FIGURE 6

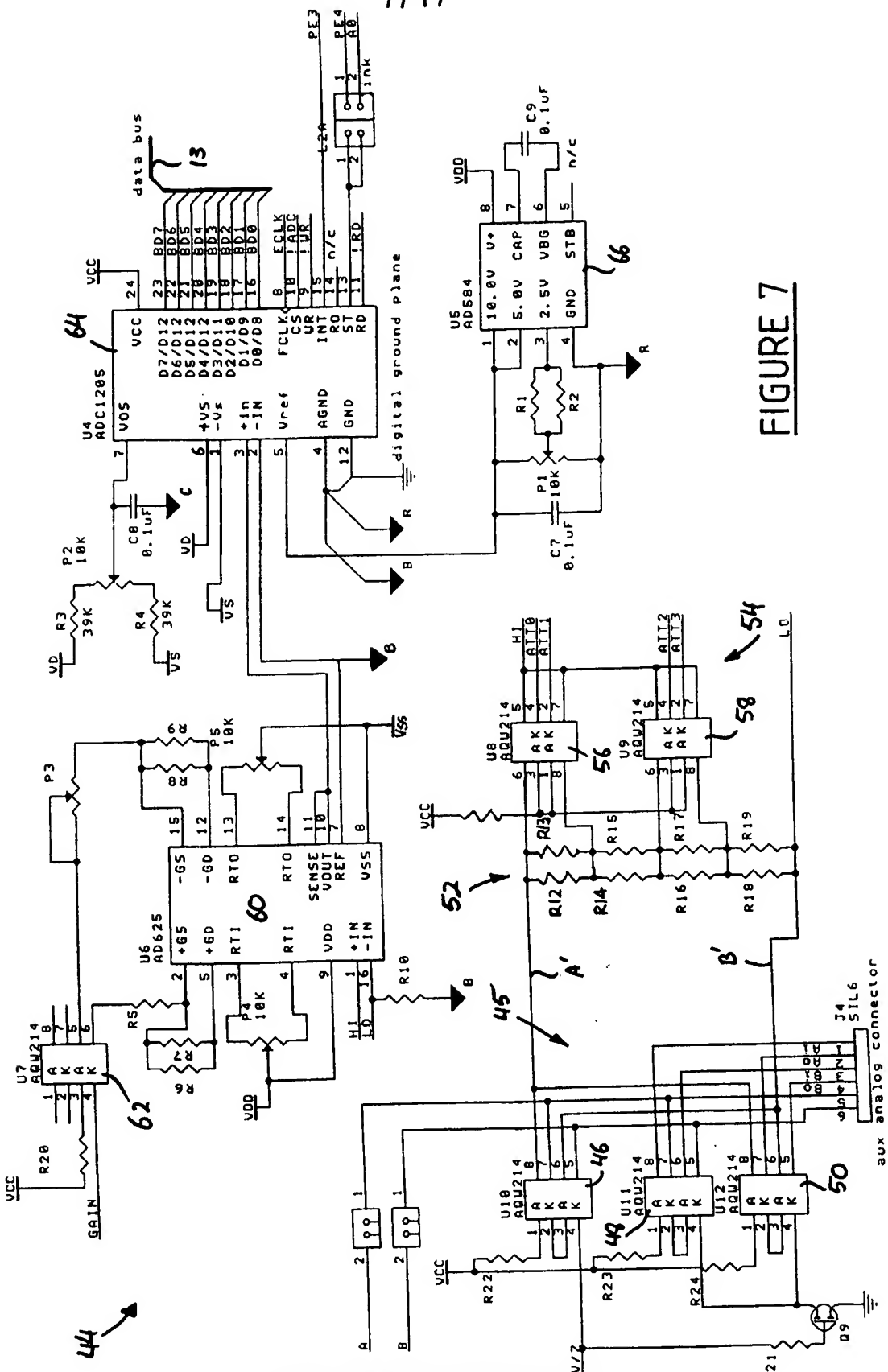
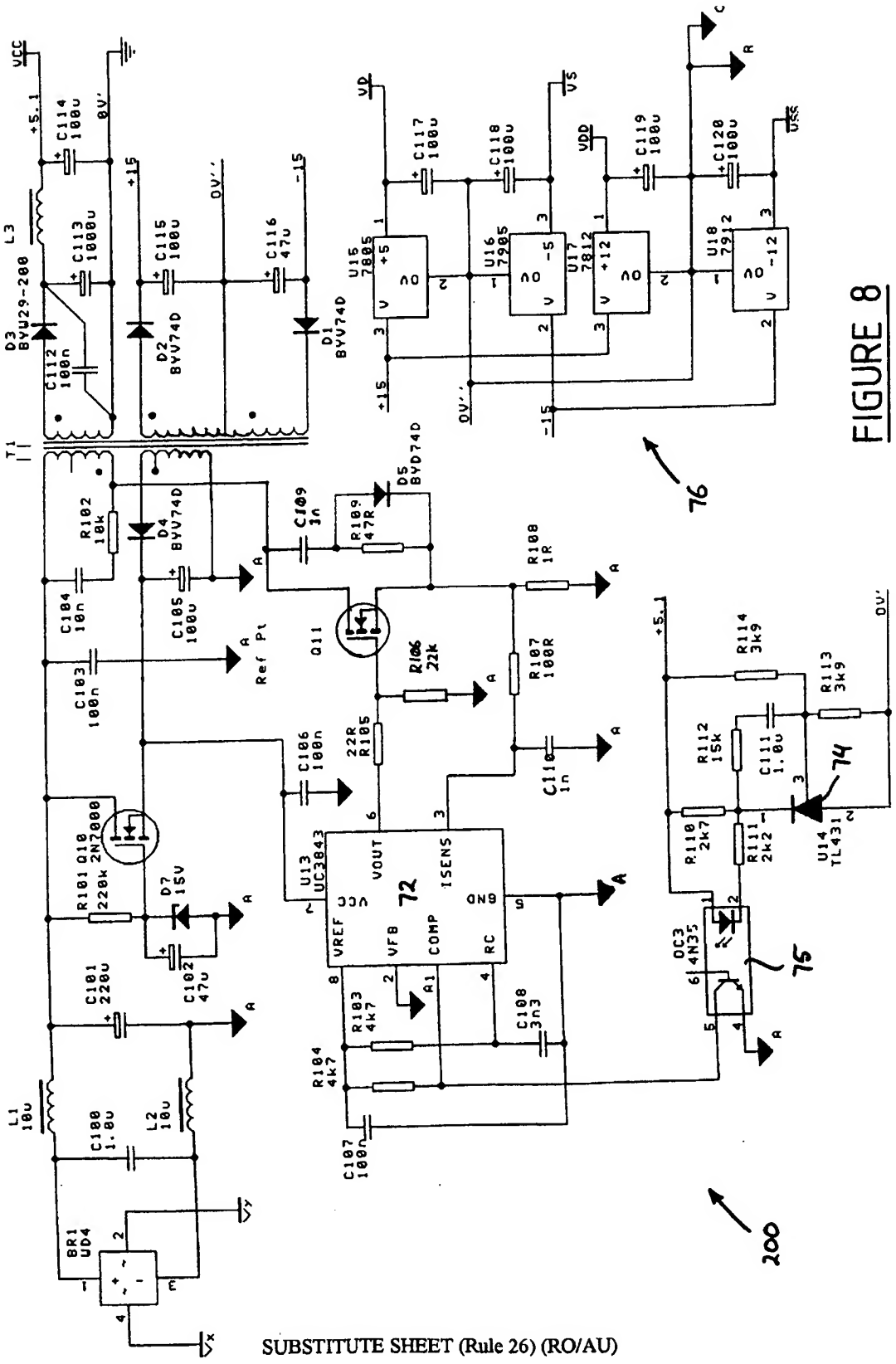

data bus
13
digital ground plane
U4 ADC1205
U5 AD584
U6 AD625
U7 AQU214
U8 AQU214
U9 AQU214
U10 AQU214
U11 AQU214
U12 AQU214
J4 SIL6
aux analog connector
GAIN
44
45
46
49
50
52
54
56
58
60
62
64
66

FIGURE 7


VCC
+5.1
0V'
+15
0V''
-15
L3
T1
D3 BYV29-200
D2 BYV74D
D1 BYV74D
D4 BYV74D
D5 BYD74D
C112 100n
C113 1000u
C114 100u
C115 100u
C116 47u
C117 100u
C118 100u
C119 100u
C120 100u
U15 7805 +5
U16 7905 -5
U17 7812 +12
U18 7912 -12
VD
VS
VDD
VSS
C
R
76
R102 10k
C104 10n
C105 100u
C109 1n
R109 47R
R108 1R
R106 22k
R107 100R
Q11
Ref Pt
C103 100n
R105 22R
C106 100n
C110 1n
R101 220k
Q10 2N7000
D7 15V
C102 47u
C101 220u
U13 UC3843
VREF
VFB
COMP
VOUT
ISENS
GND
VCC
72
R103 4k7
R104 4k7
C108 3n3
C107 100n
L1 10u
L2 10u
C100 1.0u
BR1 UD4
R114 3k9
R113 3k9
R112 15k
C111 1.0u
R110 2k7
R111 2k2
U14 TL431
74
OC3 4N35
75
200
FIGURE 8

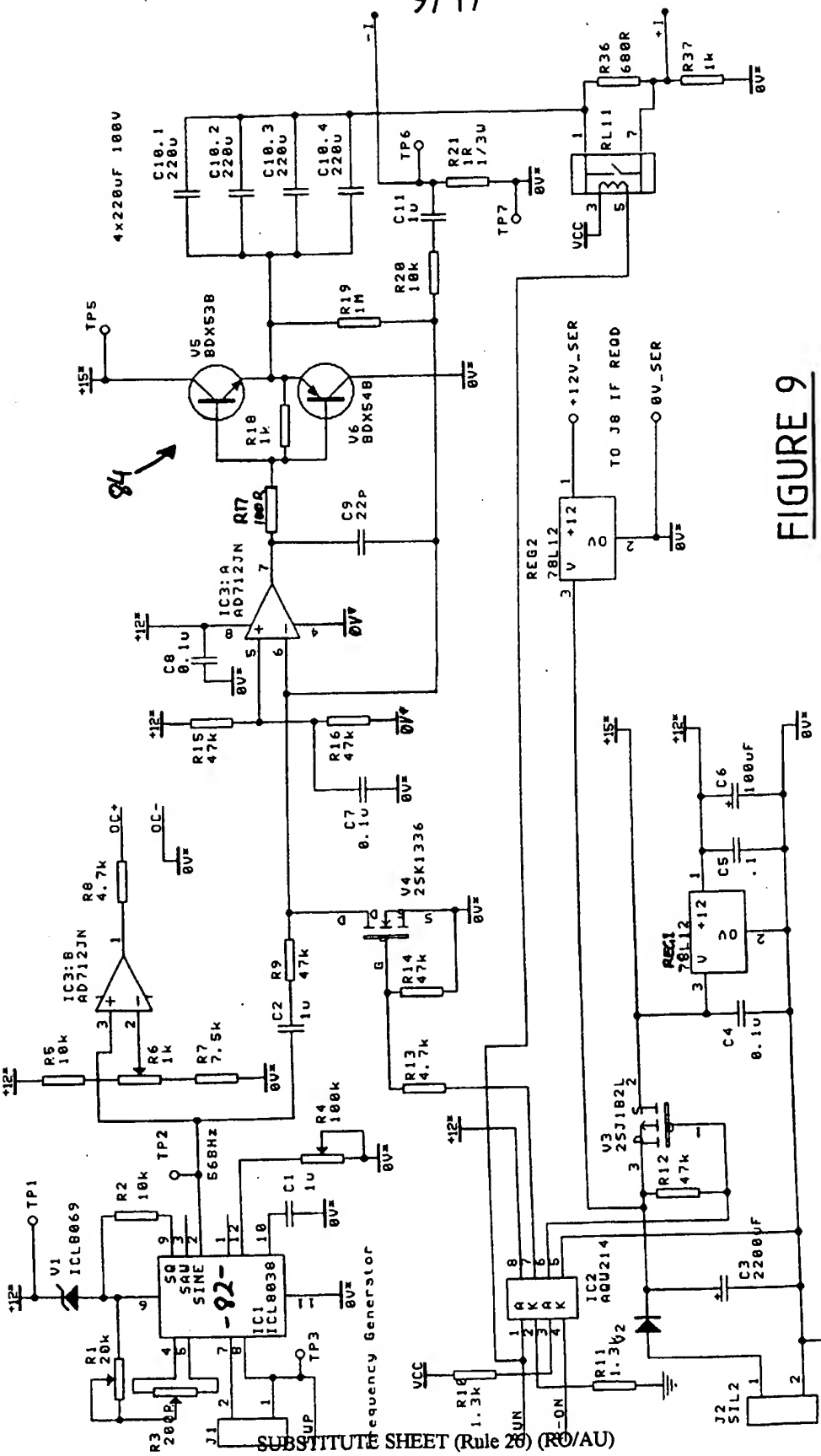

4x220uF 100V
C10.1 220u
C10.2 220u
C10.3 220u
C10.4 220u
C11 1u
TP6
TP7
R21 1R 1/3W
R36 680R
R37 1k
RL11
VCC
R20 10k
R19 1M
TP5
V5 BDX53B
V6 BDX54B
R18 1k
R17
C9 22P
IC3:A AD712JN
C8 0.1u
R15 47k
R16 47k
C7 0.1u
REG2 78L12
+12V_SER
0V_SER
TO J8 IF REQD
REG1 78L12
C6 100uF
C5 .1
C4 0.1u
V4 2SK1336
R14 47k
R13 4.7k
R8 4.7k
IC3:B AD712JN
R9 47k
C2 1u
R5 10k
R6 1k
R7 7.5k
R4 100k
C1 1u
TP2
568Hz
V3 2SJ182L
R12 47k
R2 10k
TP1
V1 ICL8069
IC1 ICL8038
SQ SAW SINE
-92-
IC2 AQU214
C3 2200uF
TP4
R1 20k
R3 200R
TP3
J1
UP
DN
R10 1.3k
R11 1.3k
J2 SIL2
Frequency Generator
84
90

FIGURE 9

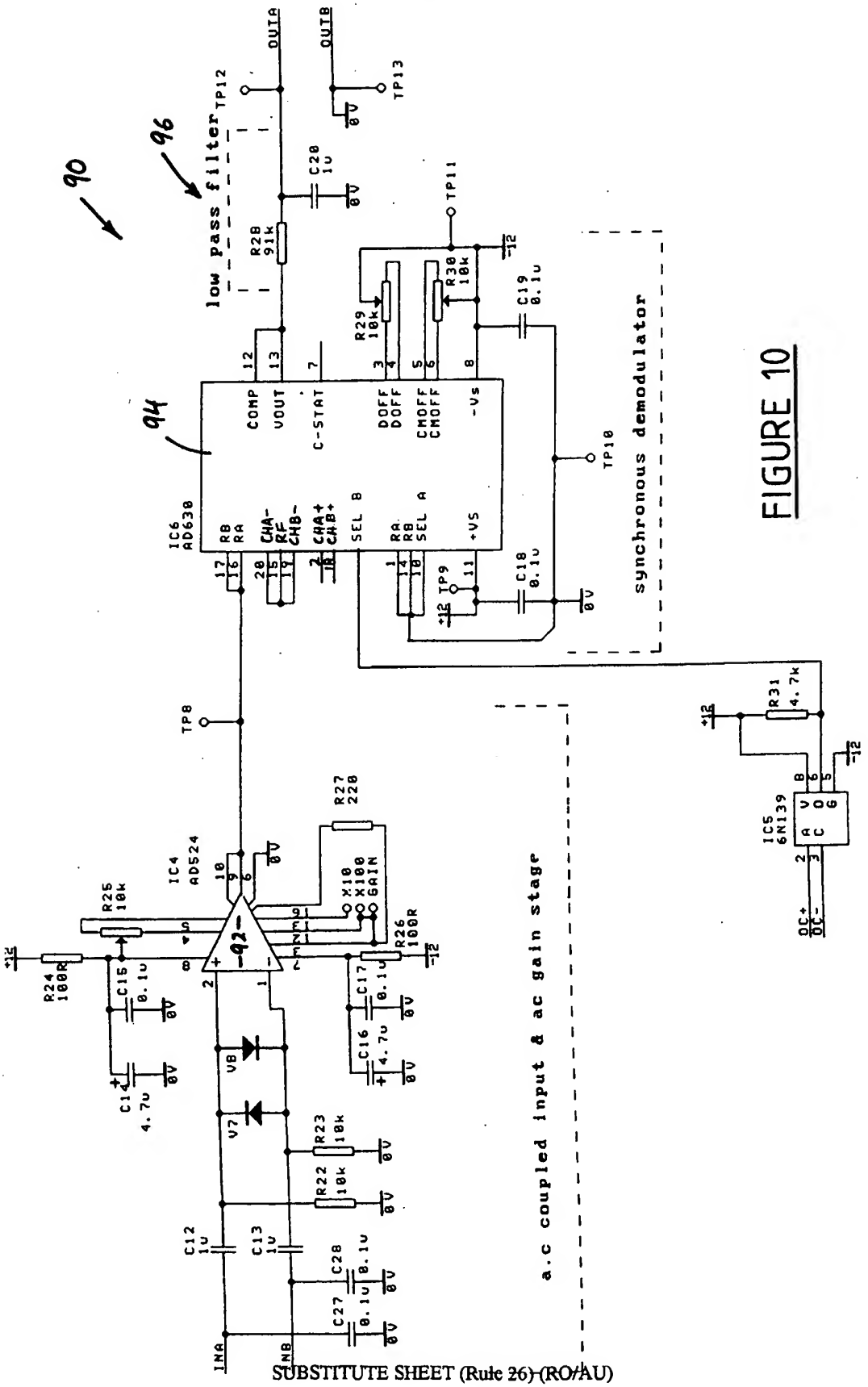

90
96
94
low pass filter
synchronous demodulator
a.c coupled input & ac gain stage
IC6 AD630
IC4 AD524
IC5 6N139
OUTA
OUTB
TP12
TP13
TP11
TP10
TP9
TP8
R28 91k
R29 10k
R30 10k
R31 4.7k
R27 220
R25 10k
R26 100R
R24 100R
R23 10k
R22 10k
C20 1u
C19 0.1u
C18 0.1u
C15 0.1u
C17 0.1u
C16 4.7u
C14 4.7u
C12 1u
C13 1u
C28 0.1u
C27 0.1u
V8
V7
INA
INB
+12
-12
0V

FIGURE 10

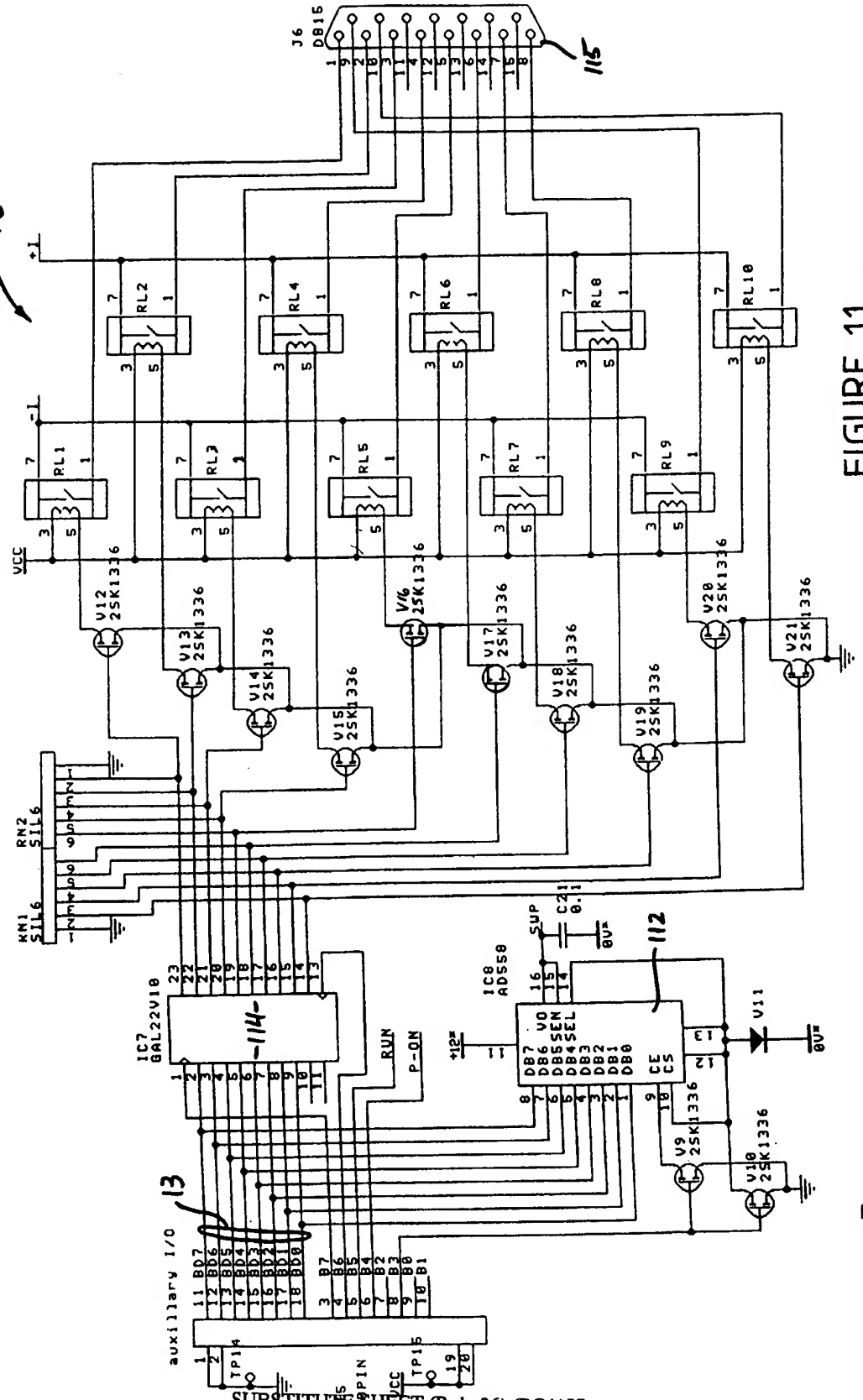

J6
DB15
115
116
+1
-1
RL1
RL2
RL3
RL4
RL5
RL6
RL7
RL8
RL9
RL10
VCC
V12 2SK1336
V13 2SK1336
V14 2SK1336
V15 2SK1336
V16 2SK1336
V17 2SK1336
V18 2SK1336
V19 2SK1336
V20 2SK1336
V21 2SK1336
RN2 SIL6
RN1 SIL6
IC7 GAL22V10
114
RUN
P-ON
IC8 AD558
SUP
C21 0.1
0V
112
+12V
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
SEN
SEL
VO
CE
CS
V11
V9 2SK1336
V10 2SK1336
13
auxillary I/O
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
B7
B6
B5
B4
B3
B2
B1
B0
TP14
TP15
PIN
VCC
110

FIGURE 11

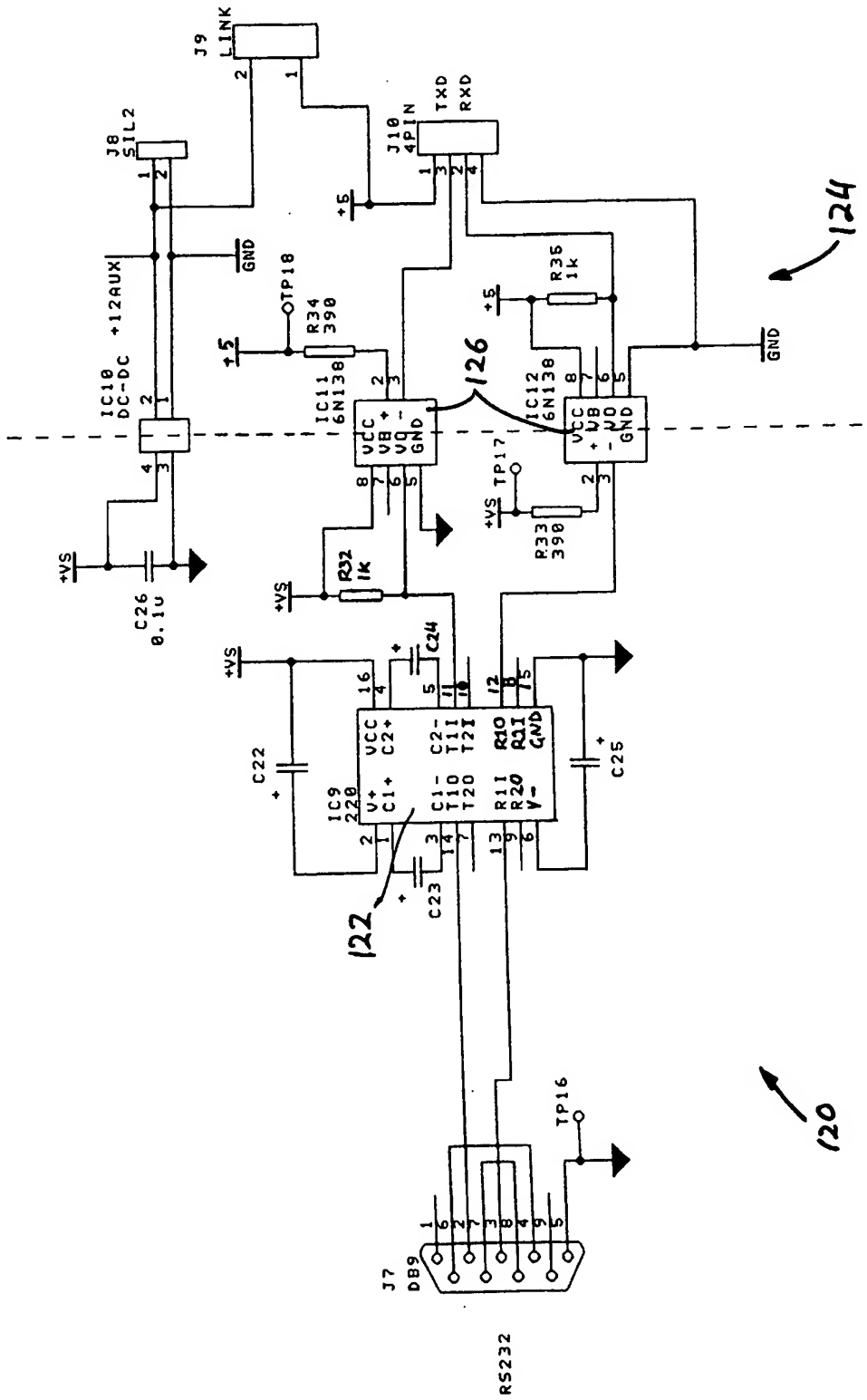

J9 LINK
J8 SIL2
J10 4PIN
TXD
RXD
+5
GND
TP18
R34 390
R35 1k
+12AUX
IC10 DC-DC
IC11 6N138
IC12 6N138
VCC
VB
VO
GND
126
124
TP17
+VS
R33 390
R32 1K
C26 0.1u
C24
C22
C25
C23
IC9 220
V+ C1+ C2+ VCC C2- T1I R1O R1I GND
C1- T1O T2O R1I R2O V-
122
TP16
J7 DB9
RS232
120

FIGURE 12

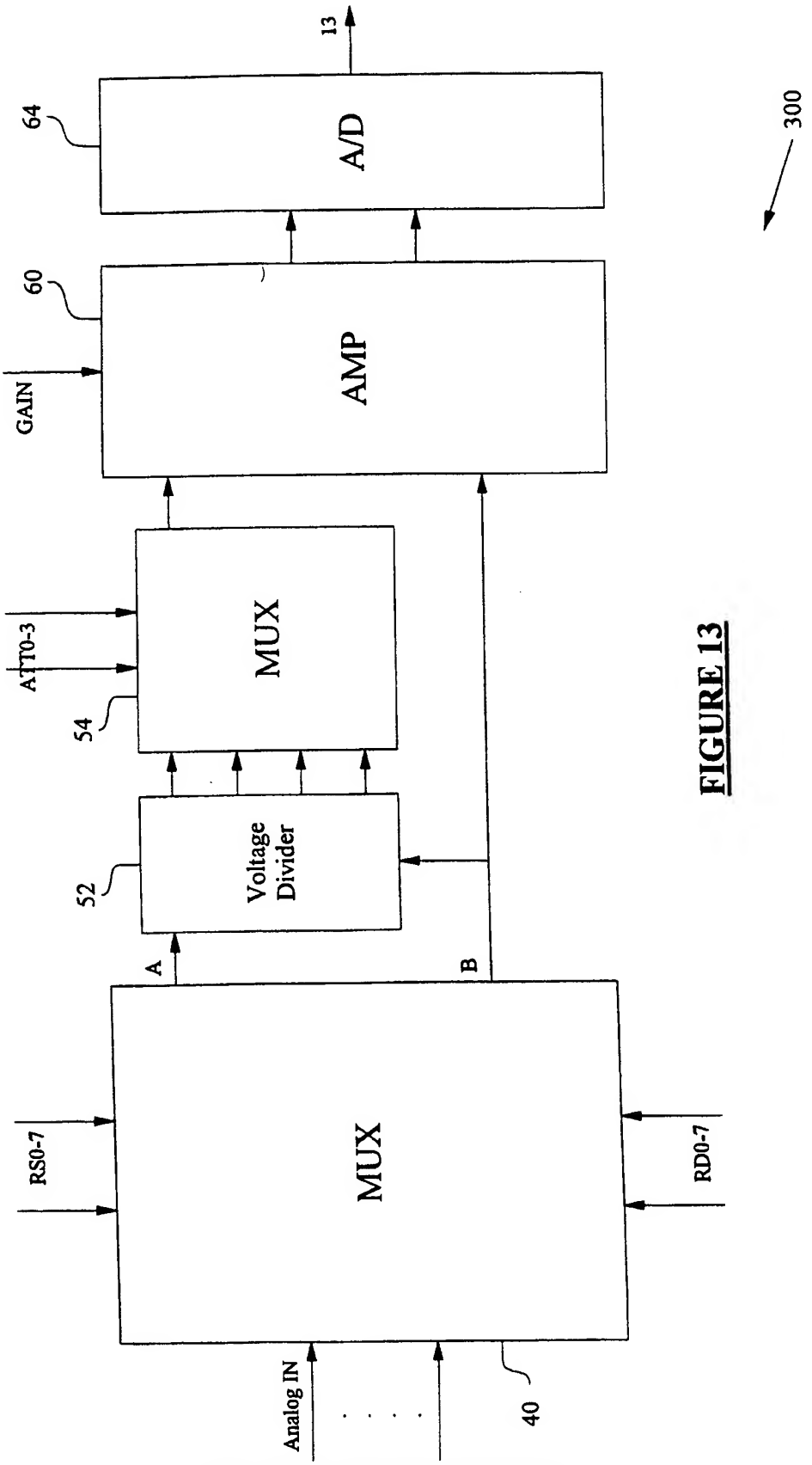

13
64
A/D
300
60
AMP
GAIN
ATT0-3
MUX
54
52
Voltage Divider
A
B
RS0-7
MUX
RD0-7
Analog IN
40

FIGURE 13

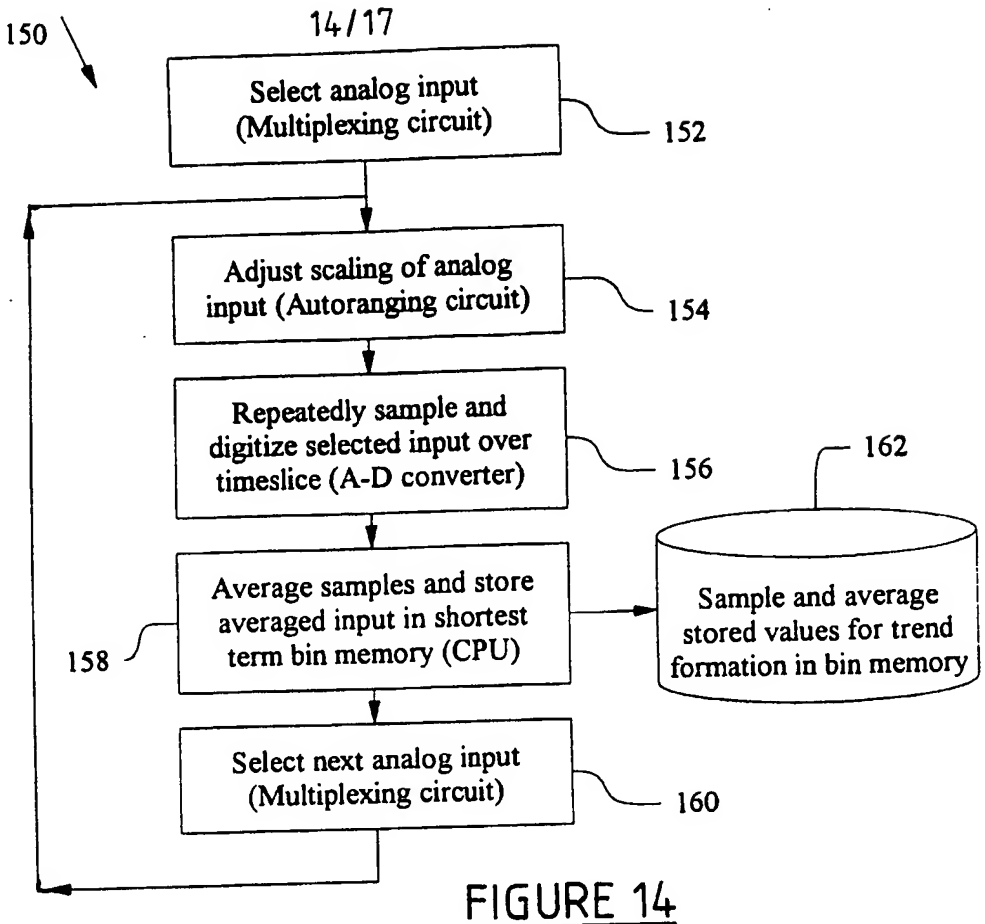


FIGURE 14

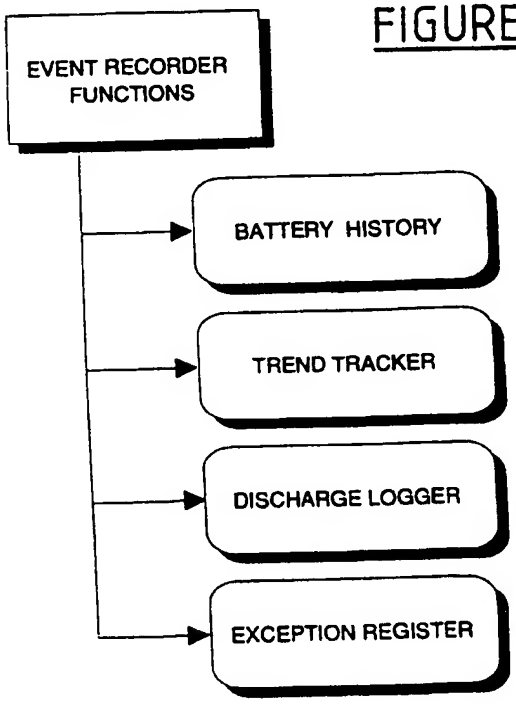


FIGURE 16

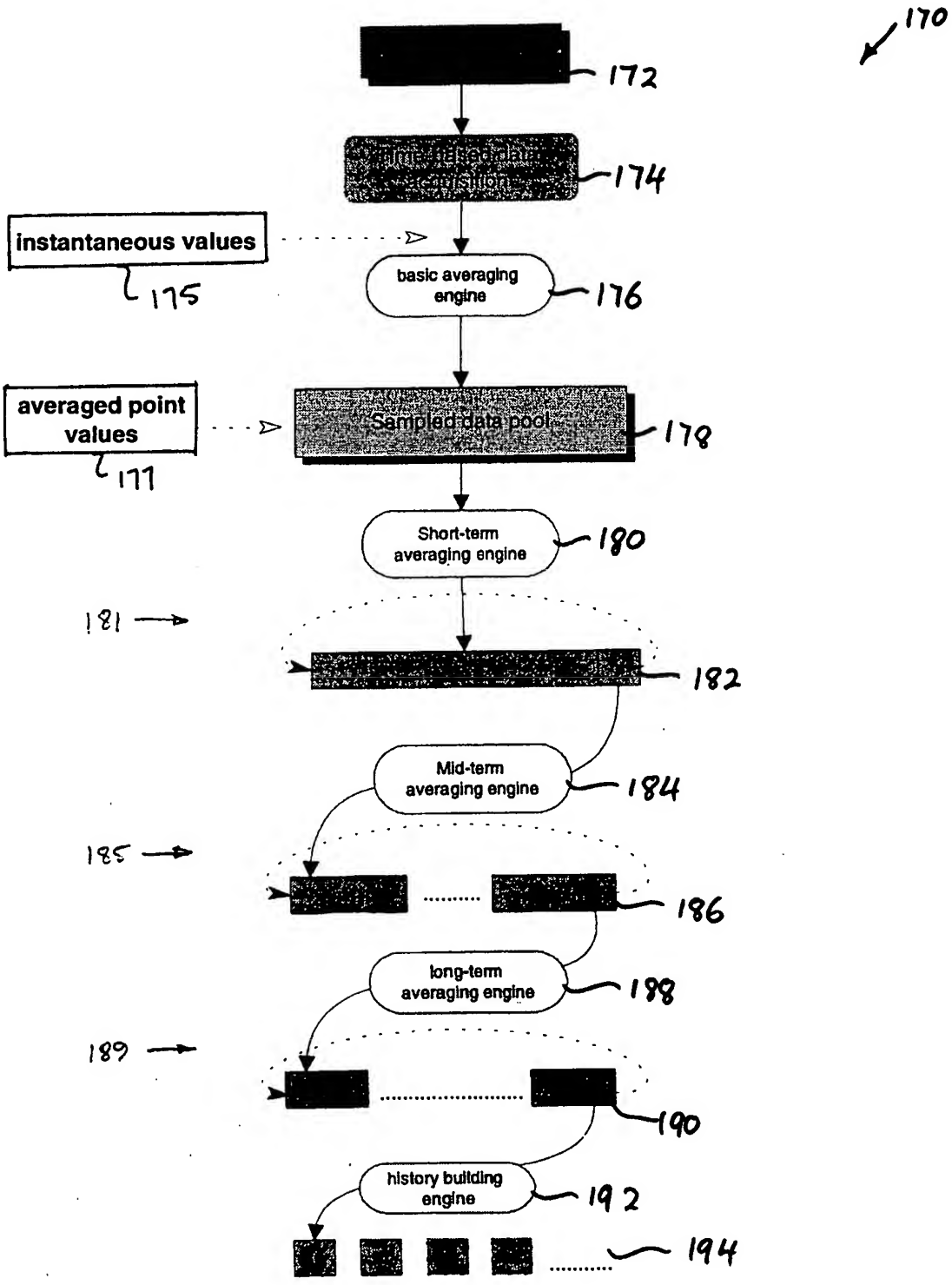

170
172
174
instantaneous values
175
basic averaging engine
176
averaged point values
177
Sampled data pool
178
Short-term averaging engine
180
181
182
Mid-term averaging engine
184
185
186
long-term averaging engine
188
189
190
history building engine
192
194

FIGURE 15

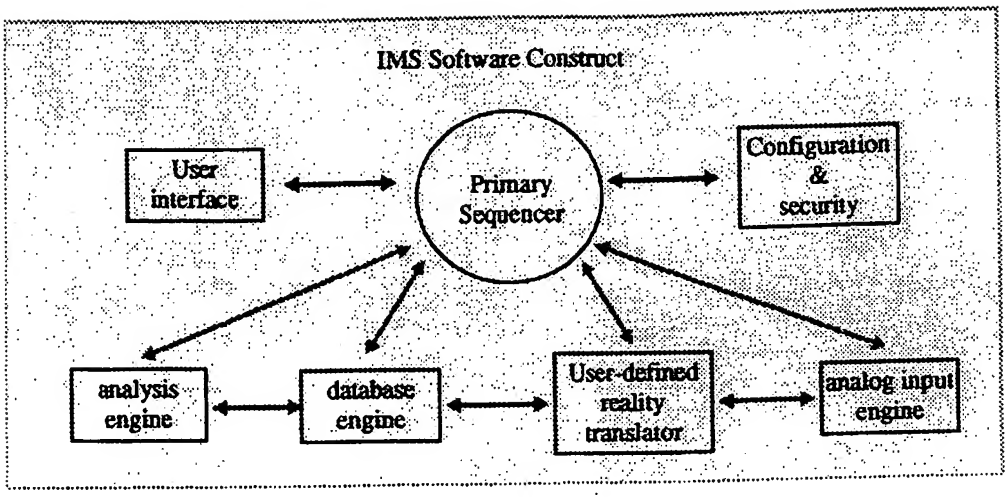

IMS Software Construct
User interface
Primary Sequencer
Configuration & security
analysis engine
database engine
User-defined reality translator
analog input engine

FIGURE 17

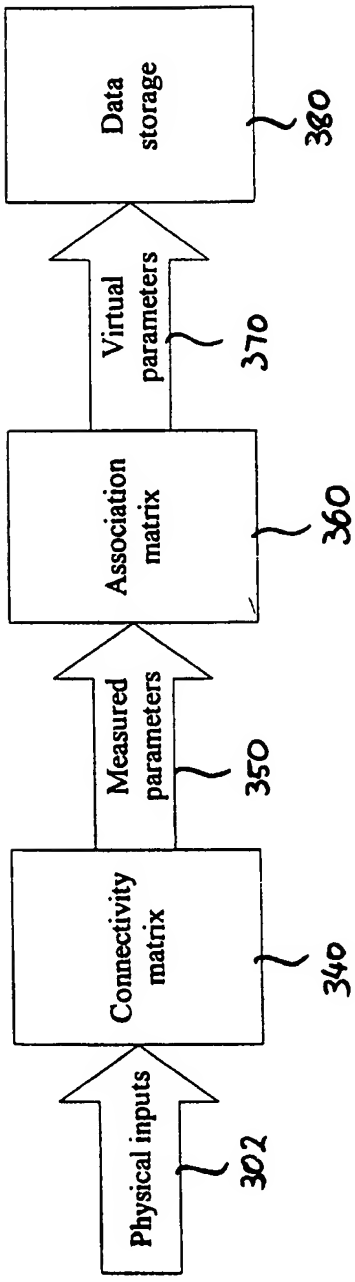

Physical inputs
302
Connectivity matrix
340
Measured parameters
350
Association matrix
360
Virtual parameters
370
Data storage
380

Figure 18

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU 98/01073

A. CLASSIFICATION OF SUBJECT MATTER

Int Cl[6]: G01R 27/02, 31/36; G06F 17/40; H01M 10/48

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: H01M, G01R, G05B, G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
AU: IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPAT : (MONITOR: or CONTROL or TEST: or CHECK:) AND ANALOG: AND DIGITAL AND MULTIPLEX: AND CONVERT: AND (STOR: or MEMORY or MANIPULAT:)
JAPIO : same as above

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	WO 94/13197 A1 (SIEMENS MEDICAL SYSTEMS INC) 23 June 1994	
X	whole document	1,7,13,25-27
Y	whole document	8-12,14-18,29,31-36
	Derwent WPAT Online Abstract Accession No: 92-081152/11 Class T01 DE 4027898 A (BRUHN, A) 5 March 1992	
X	Abstract	1,13
	US 5062101 A (DEJEWSKI) 29 October 1991	
X	whole document	1,7,13,25-27
Y	whole document	8-12,14-18,29,31-36

[X] Further documents are listed in the continuation of Box C

[X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 March 1999	11 MAR 1999
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200 WODEN ACT 2606 AUSTRALIA Facsimile No.: (02) 6285 3929	Authorized officer **MANISH RAJ** Telephone No.: (02) 6283 2175

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU 98/01073

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	EP 0277006 A2 (WESTINGHOUSE ELECTRIC CORPORATION) 3 August 1988	
X	whole document	1,7,8,13,25-27
Y	whole document	8-12,14-18,29,31-36
	GB 2188806 A (BURR-BROWN LIMITED) 7 October 1987	
X	whole document	1,7,8,13,25-27
Y	whole document	8-12,14-18,29,31-36
	Derwent WPAT Online Abstract Accession No: 86-114072/18, Class T01, T02, DE 3527952 A (INST FUR LEICHTBAU & EKO) 24 April 1986	
Y	Abstract	1,8,13,25
	EP 147239 A2 (KABUSHIKI KAISHA ISHIDA KOKI SEISAKUSHO) 3 July 1985	
X	whole document	1,7,13,25-27
Y	whole document	8-12,14-18,29,31-36
	Derwent WPAT Online Abstract Accession No: 84-310494/50, Class P31, NL 8301510 A (INNOVI N V) 16 November 1984	
Y	Abstract	14-17,27,28,30
	EP 110794 (ELECTRICITE DE FRANCE SERVICE NATIONAL) 13 June 1984	
X	whole document	1,7,8,13,25-27
Y	whole document	8-12,14-18,27-36
	EP 084610 A2 (HITACHI LTD) 3 August 1983	
X	whole document	1,7,13,25-27
Y	whole document	8-12,14-18,29,31-36

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/AU 98/01073

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
WO	94/13197	EP	673224				
DE	4027898	NONE					
US	5062101	NONE					
EP	277006	JP	1210825	US	5005142		
GB	2188806	DE	3711216	FR	2596889	JP	62242261
		US	4918647				
DE	3527952	DD	232130				
EP	147239	AU	37148/84	JP	60142215	US	4790398
NL	8301510	NONE					
EP	110794	FR	2537303				
EP	0084610	JP	58074847	US	4562545		

END OF ANNEX